MIOTA-Based Filters for Noise and Motion Artifact Reductions in Biosignal Acquisition

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ABSTRACT This paper presents a new low-voltage CMOS structure for operational transconductance amplifier (OTA) exploiting the bulk-driven, the self-cascode and the multiple-input transistor techniques (MI). The multiple-input OTA (MIOTA) circuit operates in subthreshold region using 0.5V supply voltage and offers enhanced linearity. The MIOTA is developed for biopotential signal as well as electrocardiogram (ECG) signal processing circuit and it is exploited to design a 5th-order Chebyshev low-pass and 3rd-order band-pass filters with a dynamic range (DR) of 57.6 dB and 60.4 dB, and nanopower consumption of 50 nW and 60 nW, respectively. Due to the electronic tuning of cut-off frequency, the low-pass and band-pass filters are suitable for random noise and motion artifact noise reductions in biopotential signals. The circuits were designed in Cadence environment using the standard N-well 0.18 μm TSMC CMOS technology. Intensive post-layout simulation results along with the process, voltage, temperature analysis (PVT) and Monte Carlo (MC) prove the robustness of the design. The chip area of the proposed MIOTA is 0.00725 mm^2 (118μm × 61.5 μm). Compared with standard OTA the MIOTA offers simplification of filter topology and reduced number of active elements. In order to demonstrate these advantages, the MIOTA-based filter was also build using commercially available OTA LT1228. The experimental results of OTA LT1228 confirm both the filter functionality and the advantages of the proposed MIOTA.

INDEX TERMS Bulk-driven, low-pass filter, band-pass filter, low power, low voltage, multiple input operational transconductance amplifier.

I. INTRODUCTION

Nowadays, as people become more health conscious, the growing popularity of wearable devices is the factor to stimulate the transformation toward telehealth. The wearable device also provides the wireless communication function to deliver the patient's biological data to medical professionals in real-time. Health and medical equipment must be prioritized for accuracy which is able to correctly identify the conditions of the user and diagnosis of the patient's symptoms.

Regarding to the portable and wearable devices, they become widely popular equipment in everyday life. The low-power integrated circuits are an extremely challenging topic for researchers, due to requirement of low power supply and minimal power consumption. The strict energy requirements

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must be satisfied for all subsystems such as ADC (analog-to-digital conversion) unit, computer processing, and wireless transmission. All the blocks need to work accurately and provide correct results. The portable biomedical device is an essential equipment to diagnosing a patient's disease. The ECG monitoring system is usually a 3-channel detector (multichannel system), which have the advantage of single-channel recorders being able to capture multiple leads of abnormalities at the same time as shown in Fig. 1. Electrode is identified as an acronym and has different colors: right arm (RA white), left arm (LA black), left leg (LL red), may remember: white, black and red for RA, LA and LL, respectively.

Traditional 3-channel measurement systems use differential-input instrumentation amplifier (IA) as a preamplifier to receive very small amplitude input signals and amplifying it [1]. The passive or active frequency filter
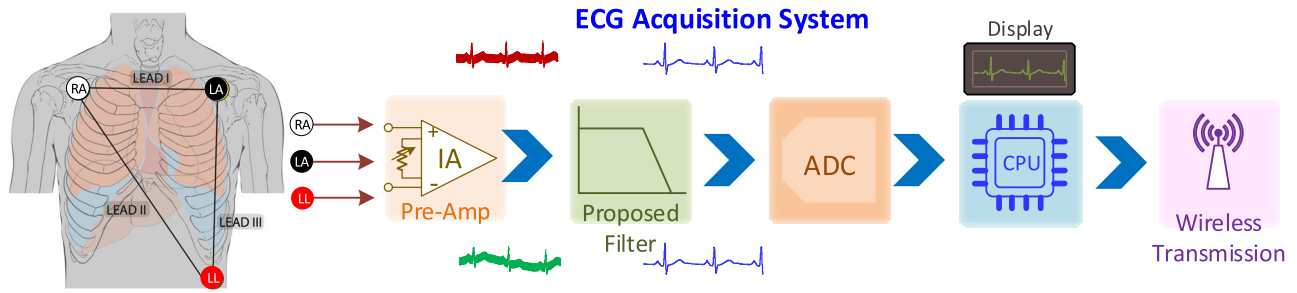
FIGURE 1. 3-lead wearable biopotential sensor.

circuits are used to remove the unwanted noise. The signals are converted into digital form by the ADC circuit. The digital signals are next processed by a central processing unit (CPU) and then the data are displayed or wireless transmitted. Because noise is amplified together with the ECG signals, a high-efficiency filter is required. Most often, the operational amplifier (OA)-based filter is used with high power supply voltage. Generally, the bio-signals are signals located in low-frequency band (below 2kHz) which are listed in Table. 1 [2]. In ECG bandwidth (0.05Hz-250Hz), the design of the RC passive filters is not effective, because it requires high resistances and large capacitances. Moreover, the passive RC circuits are difficult to realize and are not suitable for portable integrated circuits. Biosensor devices used in the past were designed using discrete components in monolithic form, that required high voltage and high power [3]. Therefore, a biosensor has been developed in the form of a SOC (system-on-chip) to combine the necessary equipment into a single chip, but the high-power consumption was required at the beginning. The CMOS circuits are widely used for low-voltage designs, exploiting operation of a MOS transistors in ohmic region [4]–[6]. Although the results are acceptable, the minimum supply voltage is still limited by the threshold voltage of MOS transistors. However, very low-voltage circuits can operate from supply voltages lower than the threshold voltage by biasing the MOS transistor in a weak inversion region [7]–[10].

Nevertheless, even for circuits operating in weak inversion, the voltage swing is limited by V_{GS} voltages of MOS transistors. To overcome the above mentioned constrains, the so-called bulk-driven technique was introduced [11], [12]. This technique can be used with sub-volt power supply and very low biasing currents in the range of nanoamps. Moreover, controlling the MOS transistors with their bulk terminals allows extending their linear range. A large number of low-voltage bulk-driven circuits devoted to different applications, have been proposed in recent years [13]–[18]. The MOS transistors operating in weak-inversion are preferred to realize low-voltage biopotential filters [19]–[23]. However, even the bulk-driven circuits in weak inversion show limitations of the voltage swing under ultra-low voltage supply.

It is worth noting that active devices with multiple-input like OTAs [31]–[34], [42]–[46] or multipath dynamic

comparators [48], [49] attracted the attention of the integrated circuit designers. It is because these devices offer the advantage of arbitrary summing or subtracting the voltage signals at the inputs, allowing topology simplification and reducing the number of used components. This is evident in applications like OTA-C filters [31]–[34], [42]–[46] or successive-approximation-register (SAR) Analog-to-Digital Converters [48], [49]. Multiple-input devices were firstly constructed by a proper parallel connection of the input transistors that create the input differential stages [31], [32]. However, this increase the count of transistors, the power consumption and the complexity of the devices. Later, multiple-input devices were obtained by multiple-input MOS transistor acquired by the capacitive divider concept using the floating-gate (MIFG) MOS transistor technique [44]–[46]. However, the MIFG becomes inappropriate for modern nano-scale CMOS technologies with gate leakage since MIFG is based on the concept of charge conservation [47]. Besides, to create the input capacitors, MIFG requires technology with double poly-silicon that limits its engaging in standard CMOS technologies with one poly-silicon. In addition, due to the charge trapped in the floating gate, the MIFG suffers from higher voltage offset than conventional gate-driven transistor. To avoid the above-mentioned disadvantages associated with MIFG, the multiple-input MOS transistor technique (MI-MOST) that based on parallel capacitive-resistance divider concept offers the solution [28]–[30]. Unlike the MIFG, the MI-MOST can be used in any standard CMOS technologies (i.e. with one poly-silicon). It has no floating gate and hence no additional technological steps are needed to eliminate the compact of the gate's trapped charge on the voltage offset.

The proposed circuit is supplied from only 0.5V, and a wide input range can be obtained with a compact structure. The circuit is devoted for low-frequency application, e.g. in biosignal detectors. To show the advantage of multiple-input, the MIOTA-C based high order low-pass (LPF) and band-pass filters (BPF) were realized for ECG signal acquisition with low-number of MIOTA. The signal flow-graph (SFG) technique with RLC ladder prototype is employed to design the active filters. The filter can be tuned through the bias currents of MIOTA. The proposed low-pass filter can remove the noise, and band-pass filter can

also reduce the low-frequency motion artifact from ECG signals.

The paper is organized as follow: Sec. II presents the high-order filter design, Sec. III describes the CMOS structure of the MIOTA, Sec. IV shows the simulation of the MIOTA based filters and Sec. V shows the experimental results of OTA LT1228 based filters. Finally, the conclusion is given in Sec. VI.

II. HIGH-ORDER FILTER DESIGN

Many design concepts, such as ladder or cascade structures can be used to realize high-order filters. Due to the low-sensitivity, the RLC ladder filter is used in this paper as a prototype. The signal flow graph (SFG) is often used to describe the filter design, which allows easy transformation of the equations to particular values of the circuit elements. It has been assumed, that the synthesized circuits will operate in a voltage mode and use only multiple-input transconductors and grounded capacitors.

A. CHEBYSHEV LADDER LOW-PASS FILTER

Fig. 2 shows the 5th-order RLC Chebyshev low-pass filter (LPF). The current and voltage are assigned in the several branches and nodes of the prototype. Using the SFG method [24], the final voltage-mode SFG can be drawn in Fig. 3.
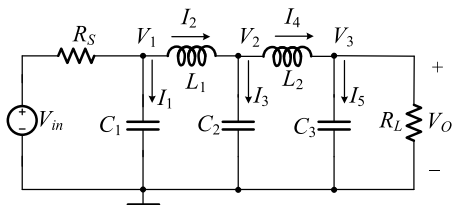

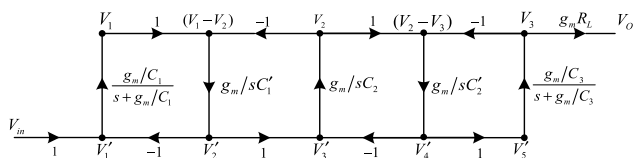**FIGURE 2. RLC 5th-order Chebyshev low-pass filter prototype.**

FIGURE 3. Voltage-mode signal flow graph of RLC low-pass filter.

The lossless and lossy integrators [50] are realized by using multiple-input OTAs and grounded capacitors as shown in Fig. 4. The transfer functions of lossless and lossy integrators can be expressed as Eq. (1) and (2), respectively.

$$V_{O1} = \sum_{i=1}^{n} (V_{+i} - V_{-i}) \frac{g_m}{sC_1} \tag{1}$$

$$V_{O2} = \sum_{i=1}^{n} (V_{+i} - V_{-i}) \frac{g_m/C_2}{s + g_m/C_2} \tag{2}$$

From the SFG in Fig. 3, the relevant branches are replaced by the lossy and lossless integrators. The completed Chebyshev 5th-order LPF can be constructed as shown in Fig. 5.
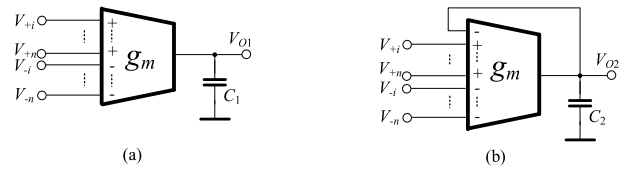

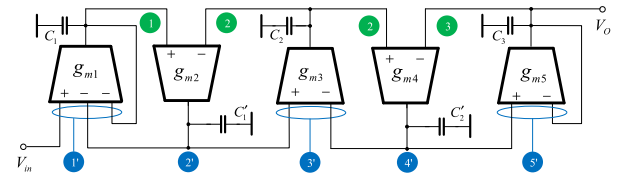**FIGURE 4. MIOTA-based integrator (a) lossless and (b) lossy.**

FIGURE 5. Voltage-mode 5th-order low-pass filter based on MIOTA-C.

B. CHEBYSHEV LADDER BAND-PASS FILTER

The motion artifact noise is usually located in very low-frequency, which is a problem of ECG signal acquisition [25]–[27]. To obtaining a clean ECG signal, the random noise and motion artifact noise at very low-frequency should be filtered out by a wide-band BPF. Fig. 6 shows the 3rd-order RLC Chebyshev band-pass filter (BPF). Using the SFG method [24], the final voltage-mode SFG can be drawn in Fig. 7.
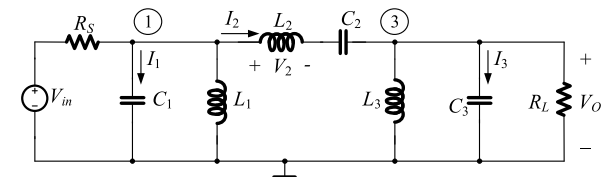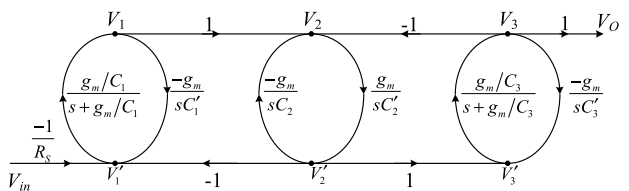

FIGURE 6. RLC Chebyshev band-pass filter prototype.

FIGURE 7. Voltage-mode signal flow graph of RLC band-pass filter.

Likewise, the relevant branches are replaced by the lossy and lossless integrators. The completed Chebyshev 3rd-order BPF can be constructed as shown in Fig. 8.
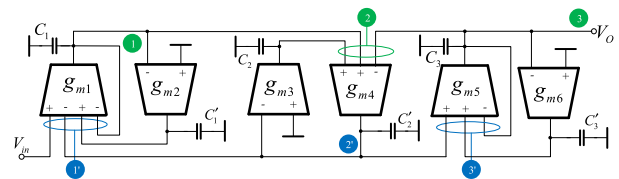

FIGURE 8. Voltage-mode Chebyshev band-pass filter based on MIOTA-C.

Moreover, passive elements of BPF was obtained from the network transformation method of LPF as shown in Fig. 6.

It consists of series and parallels LC network as shown in Fig. 9. The normal magnitude response of BPF is exhibited in Fig. 10 (gray). Regarding the bandwidth tuning, lower and upper cut-off frequency of wideband BPF ($Q \ll 1$) can be obtained by specific conditions. If the upper cutoff frequency (ω_2) is fixed, the lower cutoff frequency can be decreased ($\omega_{1n} < \omega_1$) by increasing the series capacitor ($C_{Sn} > C_S$) and parallel inductor ($L_{Pn} > L_P$) by the following condition (Case I). The magnitude response of BPF is achieved in Fig. 10 (blue).

Case I:

$$\omega_{1n} < \omega_1, \quad \omega_{0L} < \omega_0, \quad \omega_{2n} = \omega_2$$
$$C_{Sn} > C_S, \quad L_{Pn} > L_P \text{ and } L_{Sn} = L_S, \quad C_{Pn} = C_P$$

$$L_S = \frac{L_{LP}}{\omega_b} \qquad C_S = \frac{\omega_b}{\omega_0^2 L_{LP}} \qquad C_P = \frac{C_{LP}}{\omega_b} \qquad L_P = \frac{\omega_b}{\omega_0^2 C_{LP}}$$

$$\frac{1}{Q} = \frac{\omega_2 - \omega_1}{\omega_0} = \frac{\omega_b}{\omega_0} \qquad \omega_0 = \sqrt{\omega_1 \omega_2}$$
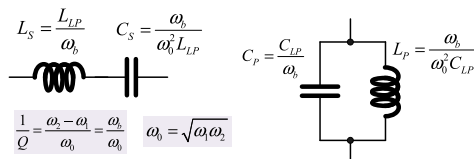
FIGURE 9. BPF passive element transformation by LPF.

On the contrary, if the lower cutoff frequency (ω_1) is fixed, the upper cutoff frequency can be increased ($\omega_{2n} > \omega_2$) by decreasing the series inductor ($L_{Sn} < L_S$) and parallel capacitor ($C_{Pn} < C_P$) by the following condition (Case II). The magnitude response of BPF is achieved in Fig. 10 (brown).

Case II:

$$\omega_{1n} = \omega_1, \quad \omega_{0R} > \omega_0, \quad \omega_{2n} > \omega_2$$
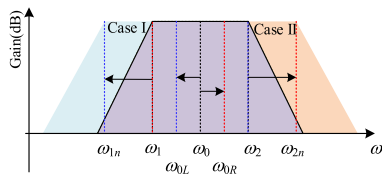$$L_{Sn} < L_S, \quad C_{Pn} < C_P \text{ and } C_{Sn} = C_S, \quad L_{Pn} = L_P$$

FIGURE 10. Bandwidth tuning of band-pass filter.

According to the bandwidth tuning technique, the BPF based on MIOTA-C in Fig. 8 can be tuned through the bias current of $OTA_{2,3,6}$(case I) and $OTA_{1,4,5}$(case II) with fixed all capacitors.

III. BULK-DRIVEN MIOTA

The CMOS structure of the proposed bulk-driven MIOTA is shown in Fig. 11. The input transistors utilize the multiple-input MOS transistor technique that was first presented and experimentally verified in [28], [30]. Based on this technique, a number of applications were recently presented in the literature [28]–[37]. As shown in Fig. 12, the multiple-input terminals of a MOS transistor is constructed simply by a parallel connection of n arbitrary number of input capacitor C_B along with high resistance R_{MOS} of two MOS transistors M_R connected as cut-off diode. Note, that the input capacitors
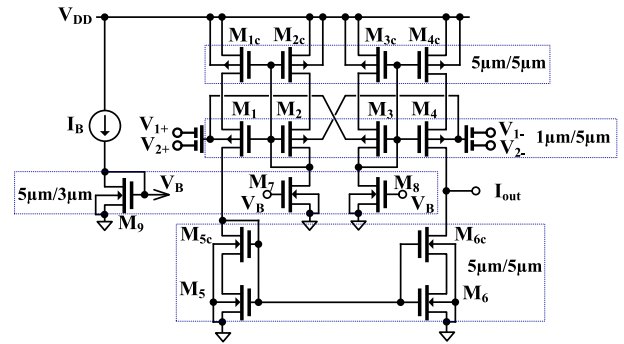
FIGURE 11. Proposed CMOS structure of the BD MIOTA.

create a voltage divider, which attenuate the signal at the inputs of "internal" OTA (i.e. OTA without multiple input), that improves the linearity of the overall structure. The high resistances R_{MOS} are used for proper DC biasing of the input terminals of the "internal" OTA.
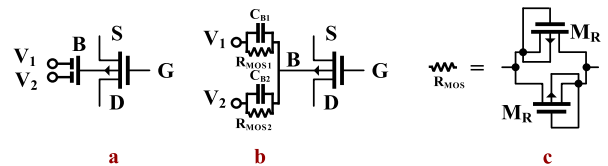
FIGURE 12. MI-BD transistor (a) symbol, (b) realization of inputs, (c) realization of R_{MOS}.

The "internal" CMOS structure of the OTA (M_1-M_8 with a biasing transistor M_9) can be seen as a modification of the non-tailed differential stage first proposed in [38]. The non-tailed architecture is suitable for ultra-low supply voltages, due to the lack of a tail current source. Despite the lack of this source, the circuit behaves as a truly differential amplifier. Neglecting the impact of second-order effects, the currents flowing through all transistors, and consequently the output current I_{out} are not sensitive to the common-mode signals, being sensitive only to the input differential signals [38]. The modification proposed here is based on replacing the transistors M_i ($i = 1 \ldots 6$) of the original circuit with self-cascode composite transistors M_i-M_{ic}, as shown in Fig. 11. Such a modification increases the linear range of the OTA, as well as increases its output resistance. The linear range is increased thanks to a negative feedback, introduced by the transistors M_{1c}-M_{4c}, operating in a triode region. Note, that the limitation of the output voltage swing due to transistors M_{1c}-M_{4c} is very small, since voltage drops across these transistors are in the range of several mV only.

Assuming operation in a weak inversion region, the drain current of a p-channel MOS can be expressed as:

$$I_D = I_T \left(\frac{W}{L} \right) \exp \left(\frac{V_{SG} + V_T}{nU_T} \right) \left[1 - \exp \left(-\frac{V_{SD}}{U_T} \right) \right] \quad (3)$$

where $I_T = 2n\mu C_{OX} U_T^2$ is the technology current, n is the subthreshold slope factor, U_T is the thermal potential, μ is

the carrier mobility, C_{OX} is the gate capacitance per unit area and V_T is the threshold voltage, which can be approximated as:

$$V_T = V_{TO} - (n - 1) V_{BS} \quad (4)$$

where V_{TO} is the threshold voltage for $V_{BS} = 0$.

Assuming the above model and fully-differential input signals, the large-signal transfer characteristic of the "internal" OTA in Fig. 11, for identical self-cascode transistors $M_{1,1c}$-$M_{4,4c}$ and $M_7 = M_8 = M_9$ can be expressed as:

$$I_{out} = 2I_B \sinh\left(\frac{\eta}{a} \cdot \frac{V_{id}}{nU_T}\right) \quad (5)$$

where $\eta = (n - 1) = g_{mb1,4}/g_{m1,4}$ and V_{id} is the input differential voltage of the "internal" OTA (between bulk terminals of M_1 and M_4). The factor a is associated with negative feedback introduced by transistors M_{1c-4c} in self-cascode transistors M_{1-4}-M_{1c-4c}. With linear approximation, which is justified by small variations of the potentials at the source terminals of transistors M_i ($i = 1..4$), it can be expressed as:

$$a = \frac{1 + (g_{mi}/g_{mic})}{(g_{mi}/g_{mic})} \quad (6)$$

In a weak inversion region this factor is equal to 2, since $g_{mi} = g_{mic}$. Note, that for the original circuit, without self-cascode connections, this factor is equal to 1.

Taking into account the input capacitive divider of the MIOTA, the large-signal characteristic from i-th input, and other inputs grounded for AC signals, can be expressed as:

$$I_{out} = 2I_B \sinh\left(\frac{\eta}{a} \cdot \frac{V_{i+} - V_{i-}}{nU_T} \cdot \frac{C_{Bi}}{C_{TOT}}\right) \quad (7)$$

where C_{Bi} is the capacitance of the i-th input and C_{TOT} is the sum of all capacitances of the input capacitive divider and the input capacitance of the "internal" OTA C_{in}. Note that assuming $C_{Bi} \gg C_{in}$, the impact of C_{in} can be neglected.

From (7), the third-order harmonic distortion (HD$_3$) can be expressed as follows:

$$HD_3 = \frac{1}{24}\left(\frac{\eta}{a} \cdot \frac{C_{Bi}}{C_{TOT}}\right)^2 \cdot \left(\frac{V_{i+} - V_{i-}}{nU_T}\right)^2 \quad (8)$$

Thus, the combination of several techniques, namely, the BD approach ($\eta < 1$), the self-cascode connections ($a = 2$) and the MI approach ($C_i/C_{TOT} < 1$) extends the linear range of the MIOTA, and allows achieving sufficient linear range even in a weak inversion region. For instance, assuming $\eta = 1/3$, $C_{Bi}/C_{TOT} = 0.5$ and $nU_T = 35$mV, the HD$_3 = 1\%$ for $V_{i+} - V_{i-} = 205$ mV, which is a relatively large range for sub-0.5V circuits. Note, that for a classical BD differential pair HD$_3 = 1\%$ for $V_{i+} - V_{i-} = 18$mV$/\eta$, which is equal to 54mV for $\eta = 1/3$. The linear range will even be more extended with larger number of inputs, due to the input capacitive divider.

It is also worth noting, that according to (8), application of self-cascode connections ($a = 2$) reduces the HD$_3$ four times as compared with the classical solution without self-cascode connections ($a = 1$) for the same input voltage.

From (7) the small-signal transconductance of the MIOTA, ($a = 2$), can be calculated as a first derivative, and is equal to:

$$G_m = \frac{dI_{out}}{d(V_{i+} - V_{i-})} = \frac{I_B}{nU_T}\eta \cdot \frac{C_{Bi}}{C_{TOT}} \quad (9)$$

Since $(I_B/nU_T)\eta$ is equal to the bulk transconductance of the p-channel transistors M_1-M_4 ($g_{mb1,4}$), then:

$$G_m = g_{mb1,4} \cdot \frac{C_{Bi}}{C_{TOT}} \quad (10)$$

Thus the small-signal transconductance is reduced by the triode-operating transistors M_{1c}-M_{4c}, that can be considered as source degeneration resistors, introducing a negative feedback ($2g_{mb1,4}$ in original circuit without negative feedback [38]) and by the input capacitive divider. The transconductance can be tuned with the biasing current I_B. The low-frequency voltage gain of the MIOTA (A_{vo}) can be expressed as:

$$A_{vo} = 2\frac{g_{mb1,4}}{g_{dsp} + g_{dsn}} \cdot \frac{C_{Bi}}{C_{TOT}} \quad (11)$$

The low-frequency gain of the "internal" OTA is the same as for the original circuit, since both, the input transconductance as well as the output conductance are reduced in the same proportion. However, the input capacitive divider reduces the voltage gain of the MIOTA, since it further reduces the input transconductance of the circuit.

Assuming for simplicity that the subthreshold slope factors of p- and n-channel MOS transistors are equal to each other, the input referred thermal noise of the OTA can be expressed in the following simple form:

$$\overline{v_n^2} = \frac{6\overline{i_n^2}}{g_{mb1,4}^2} \cdot \left(\frac{C_{TOT}}{C_{Bi}}\right)^2 \quad (12)$$

where:

$$\overline{i_n^2} = 28kT\frac{I_B}{nU_T} \quad (13)$$

Hence, the input capacitive divider increases the input referred noise in the same proportion, as extends the linear range, that suggest, that it does not affect the dynamic range. However, if the MIOTA would be realized as a connection of n OTAs, each biased with n-times lower current, then such a circuit would have lower dynamic range than the approach based on the input capacitive divider [31].

It is worth noting that despite of using the bulk-driven and multiple-input techniques, the proposed circuit in Fig. 11 has the advantage of being applicable in any standard CMOS technology. Note, that the bulk terminal of only one type of transistor (PMOS in case of N-well technology) is used as input terminal. Also, the input capacitors that create the multiple-inputs are also standard one that are available in any CMOS technology.

IV. SIMULATION RESULTS

The proposed circuits were designed and verified in Cadence environment using the 0.18 μm CMOS technology from TSMC. Intensive post-layout simulation results along with the process, voltage, temperature analysis (PVT) and Monte Carlo (MC) are presented in this section to prove the robustness of the design. The voltage supply was 0.5 V. The transistor aspect ratio of the MIOTA are depicted in Fig. 11. The input capacitors of the MIOTA are high-linear metal insulator metal capacitor (MIM) available in TSMC technology and each has a 0.5 pF. This capacitor value was selected based on post-layout simulation in order to minimize its value and hence the chip area from one side and to minimize the influence of the parasitic capacitances of the other components on the circuit performance from side other. The transistor M_R has W/L = 4μm/5μm. Note, that since M_R is based on PMOS transistors operating in cut-off region the value of this resistance is quite high (GΩ range) even with minimum transistor dimension. The layout of the proposed MIOTA is shown in Fig. 13. The chip area is 0.00725 mm^2 (118μm $\times$ 61.5 μm).
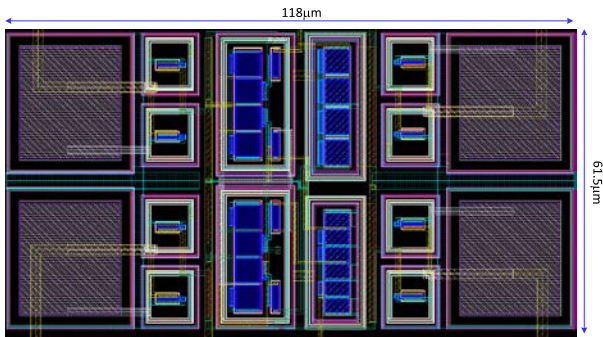
FIGURE 13. Layout of the proposed MIOTA circuit.

Fig. 14. (a) shows the DC transfer characteristics of the proposed BD-MIOTA, the circuit shows good linearity in the range of $\pm$ 0.3 V.
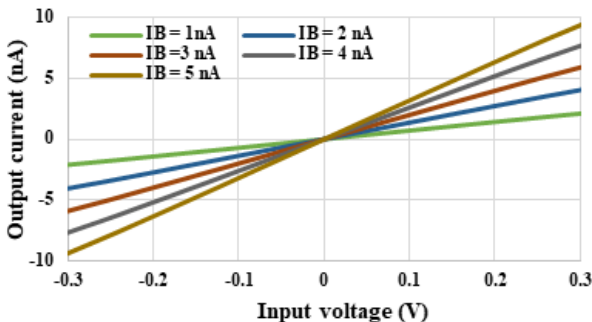

FIGURE 14. DC transfer characteristic of the BD-MIOTA.

The transient response of the MIOTA for a sine wave input signal with 300mV$_{pp}$ @ 10Hz applied to the input while the output is grounded is shown in Fig. 15(a). The output signal spectrum in Fig. 15 (b) shows that the third harmonic HD3 is lower than the fundamental by 54.89dB and the total harmonic distortion (THD) was 0.18%.
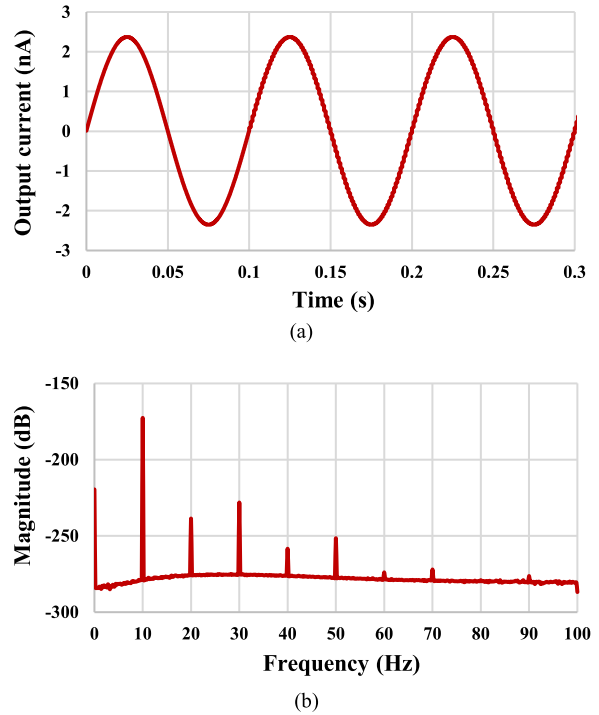

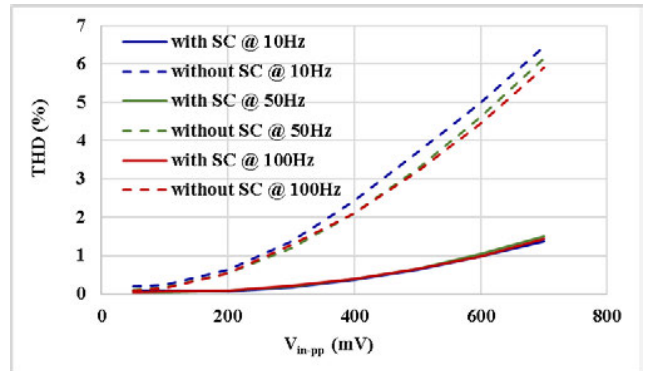**FIGURE 15.** (a) transient analysis of the output signal (b) the signal spectrum.

FIGURE 16. THD of the MIOTA with and without self-cascode transistors for different input signal values and different frequencies.

The THD versus V$_{in-pp}$ and different frequencies: 10Hz, 50Hz, 100Hz for the proposed MIOTA with and without self-cascode (SC) transistors is shown in Fig. 16. It is evident that the circuit with self-cascode transistor offers much lower THD even below 1% for 500mV$_{pp}$ that confirm the good linearity of the circuit. Note, that the THD ($\approx$ HD$_3$) for the version with self-cascode connections is approximately 4 times lower than for the version without self-cascode, for the same input voltages, which agrees with (8). The basic performance of the MIOTA-based integrator (with two inputs), with 20 pF load capacitance and I_B = 5nA are shown in Table 1.

The value of the passive elements of the RLC prototypes shown in Figs. 2 and 6 and the proposed LPF and the BPF shown in Figs. 5 and 8 are listed in Table 2.

TABLE 1. The performance of the miota-based integrator.

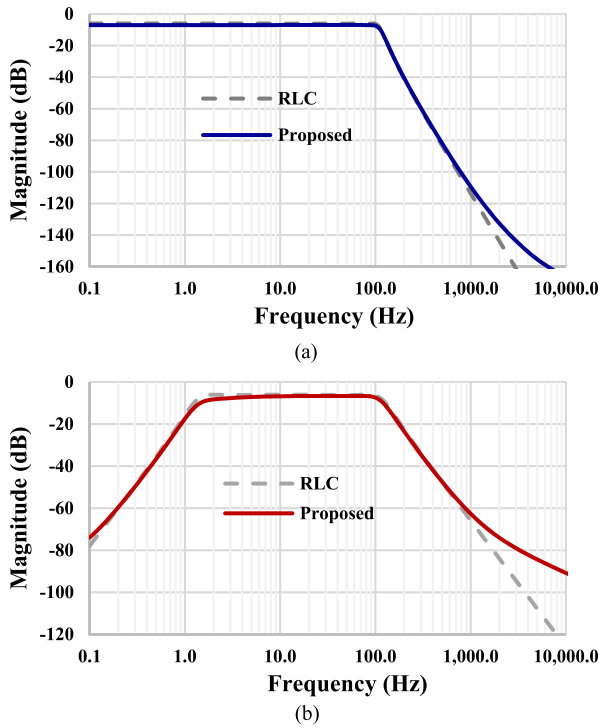|	
Gain [dB]	28.1
Phase shift [°]	88.7
Cut-off frequency [Hz]	126.3
Common mode rejection ratio (CMRR) [dB]	55.22
Power supply rejection ratio (PSRR) [dB]	33.9

TABLE 2. The passive element used in the RLC prototype and proposed filters.

	LPF	BPF
Prototype	$R_S=R_L= 1$ $C_1 = C_3 = 1.8mF$ $C_2 =3.2mF, L_1 = L_2 = 2.2mH$	$R_S=R_L= 1$ $C_1 = C_3 = 2mF$ $L_1 = L_3 = 80mH$ $C_2 = 80mF, L_2 = 2mH$
MIOTA	$C_1 = C_3 = 18p$ $C_2=32p, C'_1=C'_2 = 22p$	$C_1 =C'_2 = C_3 = 20p$ $C'_1=C_2 =C'_3 =0.8n$
LT1228	$C_1 = C_3 =5.6\mu F$ $C_2=10 \mu F, C'_1=C'_2 = 6.8\mu F$	$C_1 = C'_2 = C_3 = 0.1\mu F$ $C'_1=C_2=C'_3=20\mu F$

FIGURE 17. Magnitude responses of proposed (a) LPF with RLC (b) BPF with the RLC.
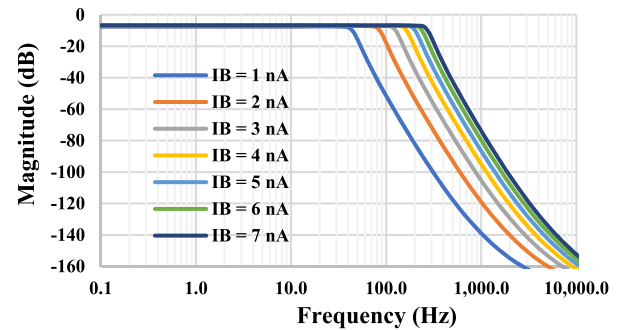

FIGURE 18. Magnitude responses of proposed LPF with different I_B.
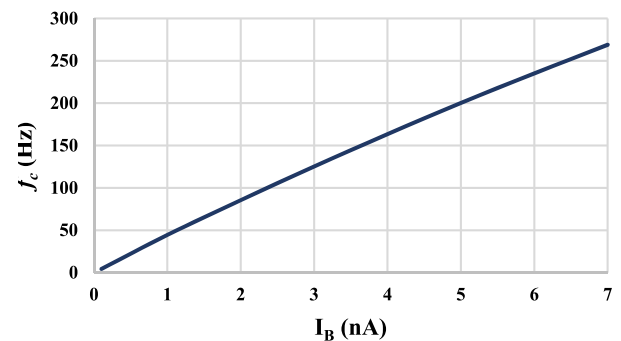
FIGURE 19. Linear relation between the cutoff frequency of the LPF and the I_B.

Note that MIOTA-based BPF has been derived from the RLC prototype with two significant poles (low- and high-frequencies). The low-frequency pole requires a large capacitor (0.8nF). The off-chip capacitors used for the BPF are recommended. The magnitude responses of the RLC prototypes and the proposed LPF and BPF are shown in Fig. 17 (a) and (b), respectively. For LPF the bias current I_B, used to set the g_m value of all OTAs, was selected 2.67 nA to achieve same cutoff frequent as the RLC prototype which is $f_c = 112$ Hz, both curves are in good agreement. For BPF two bias currents are used I_{B1} used to set the g_m value of OTA$_{1,4,5}$ and I_{B2} used to set the g_m value of OTA$_{2,3,6}$. The bias currents were selected as $I_{B1} = 2.6$ nA, $I_{B2} = 2.1$ nA to achieve bandwidth (BW) around 111 Hz for the proposed BPF. The lower cutoff frequency (f_L) was 1.3 Hz and 1.6 Hz and the upper cutoff frequency (f_H) was 120 Hz and 113 Hz for the RLC prototype and the proposed BPF, respectively.

Fig. 18 shows the magnitude responses of the proposed LPF for different bias current $I_B = 1$nA to 7 nA. The tunability and the linear relation of the cut-off frequency and I_B is confirmed in Fig. 19.

The capability of tuning the lower and/or upper cutoff frequency of the BPF is shown in Fig. 20. For Fig. 20 (a) the bias current I_{B2} was varied from 1 nA till 7 nA while I_{B1} was fixed at 5 nA, while in Fig. 20(b) the bias current I_{B1} was varied from 1 nA till 7 nA while I_{B2} was fixed at 5 nA. Fig. 20 (c) the bias current $I_{B1} = I_{B2}$ was varied from 1 nA till 7 nA. The wide tunability of the cutoff frequency is evident in all cases.

The process, voltage, temperature (PVT) corner analyses of the LPF with $I_B = 5$nA and the BPF with $I_{B1} = I_{B2} = 5$nA were provided with MOS transistor corners: slow-slow, slow-fast, fast-slow and fast-fast, MIM capacitor: slow, fast, the voltage supply rail corners $\pm$ 10mV, and the temperature corners: -10°C, 55°C. The results of the PVT corners of the LPF and BPF are shown in Fig. 21 (a) and (b), respectively, and are in acceptable range.

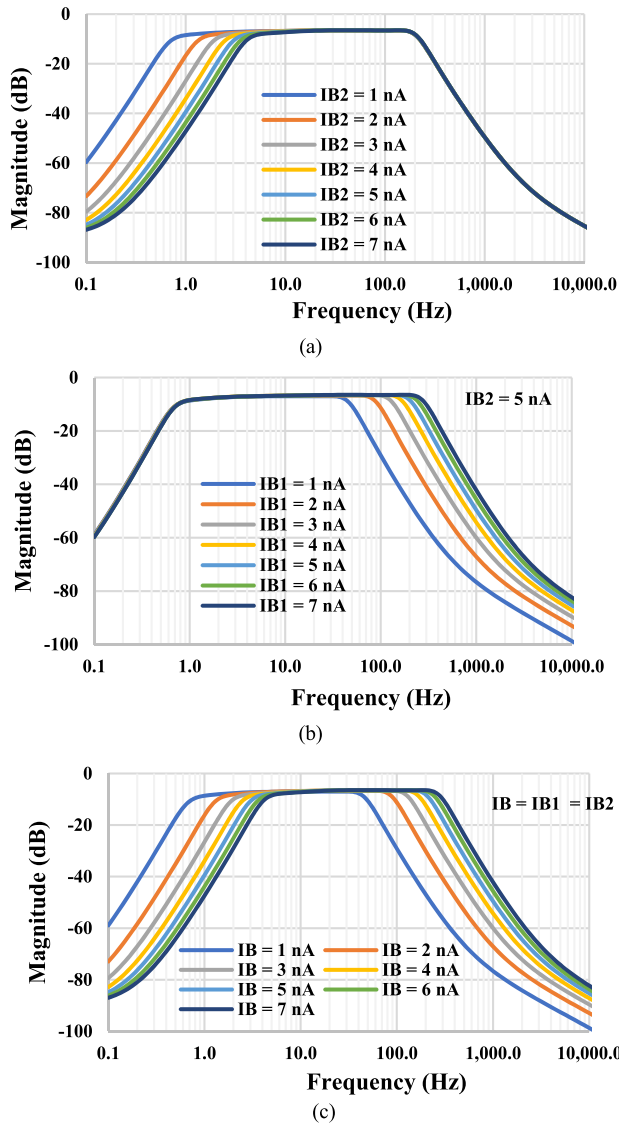To check the influence of the process and mismatch variations on the circuit functionality, the Monte Carlo analysis

FIGURE 20. Magnitude responses of proposed BPF with (a) different I_{B1} (b) different I_{B2} and (c) different $I_B = I_{B1} = I_{B2}$.

with 200 runs was provided for the gain and the cutoff frequency of the LPF with $I_B = 5nA$ and for the BPF with $I_{B1} = I_{B2} = 5nA$. The histograms of the gain of the LPF and BPF are shown in Fig. 22 (a) and (b), respectively. The gain mean value is -6.65 dB with 0.29 dB standard deviation for LPF and -6.57 dB with 0.14 dB standard deviation for BPF. The histograms of the bandwidth of the LPF and BPF are shown in Fig. 22 (c) and (d), respectively. The bandwidth mean value was 203.8 Hz with 9.79 Hz standard deviation for LPF and 209.5 Hz with 5.87 Hz standard deviation for BPF. All cases confirm the robustness of the design against process and mismatch variations.

Fig. 23 shows the transient responses of the LPF and BPF filters when a sine wave signal with 60mV peak to peak at 100 Hz was applied to the input of the filters. The total harmonic distortion was 0.62 % and 0.58 % for the LPF and BPF, respectively. The dynamic range
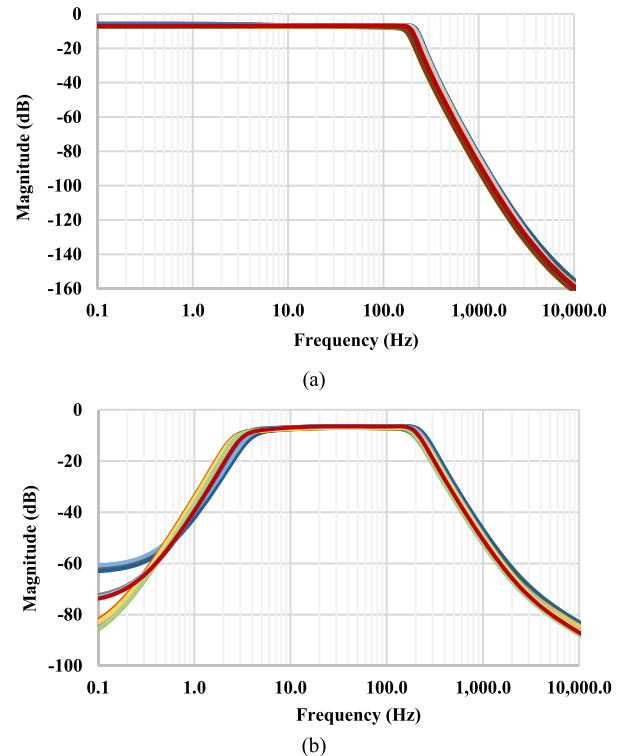

**FIGURE 21.** Magnitude responses of proposed LPF with PVT corner analysis.

$(DR = 20 \times \log(V_{rms-max}/V_{rms-noise}))$ for LPF and BPF for 1 % THD while rms noise was integrated over the filter bandwidth was calculated to be equal to 57.6 dB and 60.4 dB, respectively.

To test the LPF and the BPF for ECG signal. The ECG signal combined with random noise signal of 3 mV amplitude at 500 Hz was applied to the input of the LPF. The original ECG, the noisy ECG and the recovered ECG are shown in Fig. 24. The BPF was tested with noisy ECG signal including motion-artifact noise with 3mV at 200mHz and noise with 3 mV at 500 Hz. The noisy ECG and the recovered ECG signal are shown in Fig. 25.

Table 3 compares the proposed work with some previous related works [20]–[22], [39]–[41], where the following figure of merit (FoM) [40], has been used for better comparison: $FoM = (PV_{DD})/(Nf_cDR)$ where P, N, and f_c are the power, order, and cutoff frequency of the filter, respectively. The lower the FoM, the better the performance of the filter. It is evident that the proposed filters offer the best FOM, less number of active devices, the lowest voltage supply and the best low voltage capability from all others OTA-C based filters [20], [22], [39], [40]. Compared with filters based on cascade of two stages of transistor-level biquad flipped voltage follower (FVF) [21] and flipped source follower (FSF) [41] the proposed filter still offers better dynamic range. Note that, the cascade biquad filters are pseudo differential structures that requires additional signal conditioning at the input. The motion artifact noise can be reduced thanks to the proposed wideband ladder BPF. The fine-tuning of
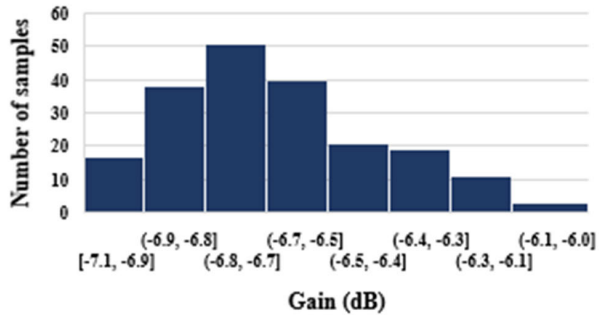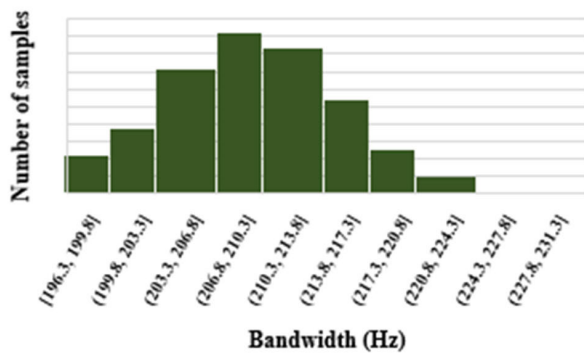
(a)
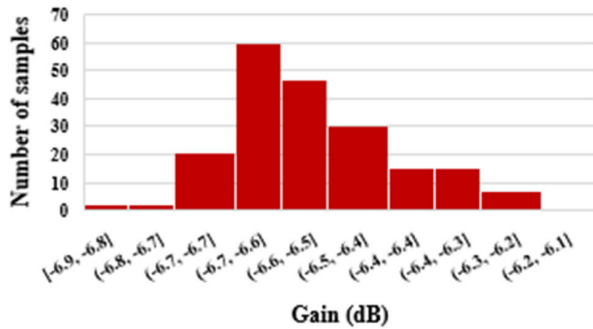
(b)
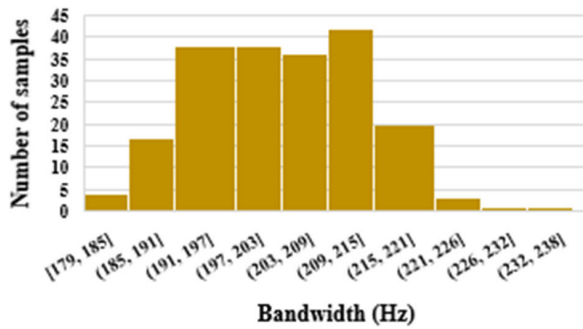
(c)

(d)

FIGURE 22. Monte Carlo analysis with 200 runs for (a) the gain of the LPF, (b) BPF, (c) the bandwidth of LPF (d) BPF.

lower and higher cutoff frequencies is another advantage offered by the proposed BPF. This, for instance, is practically required for trimming the motion artifact signal in very low frequency.
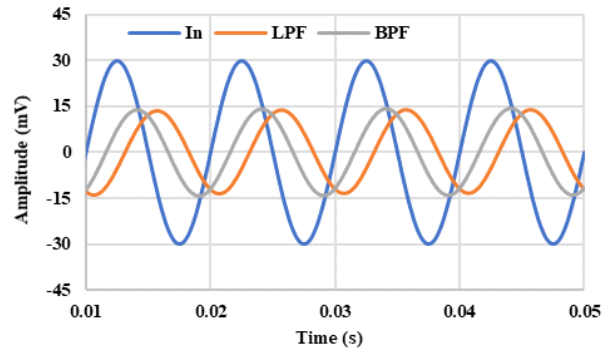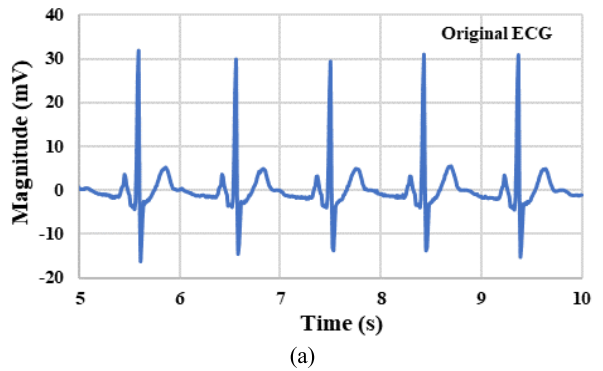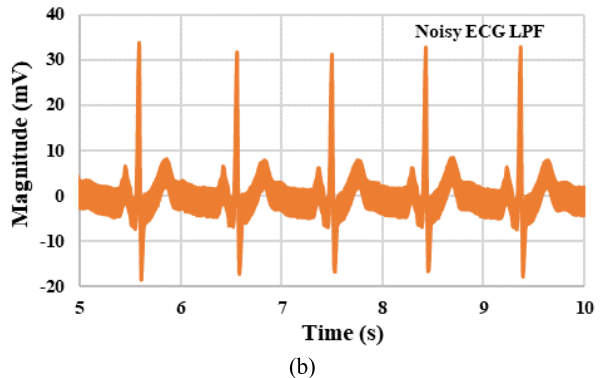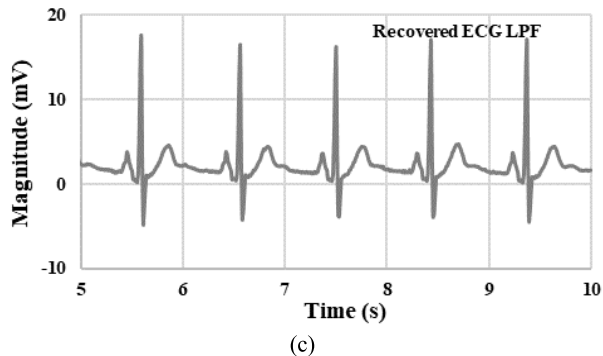

FIGURE 23. Transient response of the LPF and BPF.

(a)

(b)

(c)

FIGURE 24. Application of proposed LPF with noisy ECG signal.

V. EXPERIMENTAL RESULTS OF OTA LT1228 BASED FILTERS

The functionality of the proposed filters will be experimentally confirmed using commercially available OTAs LT1228.
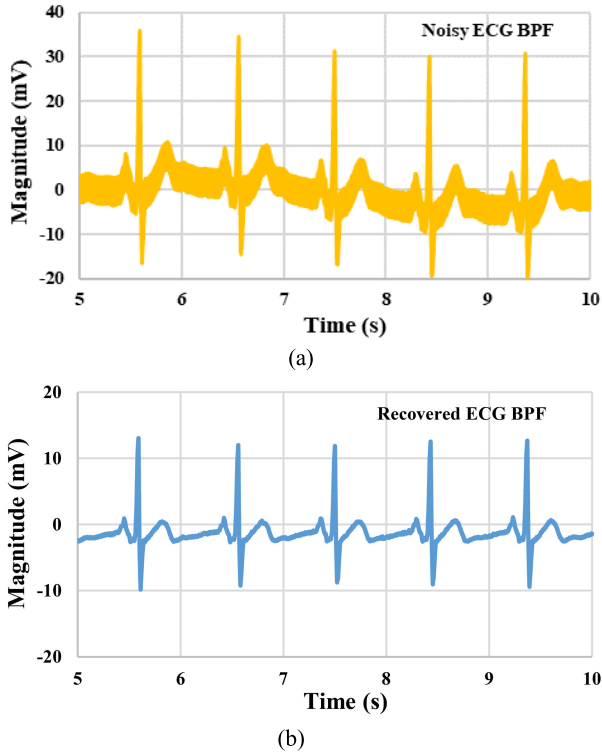
(a)

(b)

FIGURE 25. Application of proposed BPF with noisy ECG signal.

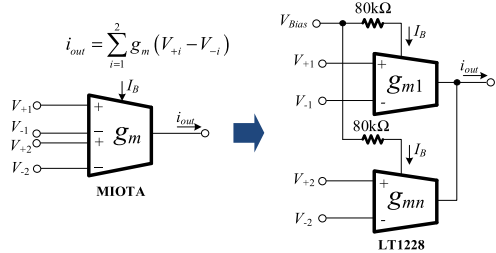$$i_{out} = \sum_{i=1}^{2} g_m \left(V_{+i} - V_{-i} \right)$$

FIGURE 26. MIOTA and MIOTA based on LT1228.

Using commercially available OTA LT1228 will also confirms the advantages of MI-OTA in term of reduced number of active elements in the filter application. The experimental setup of the proposed LPF and the BPF is provided using the off-the-shelf active and passive components. Regarding to Figs. 5 and 8, at least two differential inputs are required for MIOTA.

The MIOTA has been constructed by two commercially available OTAs LT1228 with ± 12V power supplies as shown in Fig. 26. The bias currents of OTA are controlled by V_{Bias} and 80kΩ series resistors. The capacitors of LPF and BPF are listed in Table 2. The front-end preamplifier (OTA$_A$) and final gain amplifier (OTA$_B$) have been included in the LPF and BPF as shown in Fig. 27. The ECG signal and noise are applied in the preamplifier OTA and the signals are measured after the preamplifier. Fig. 28 shows the experimental setup of LPF and BPF with ECG signal simulator (Symbio).
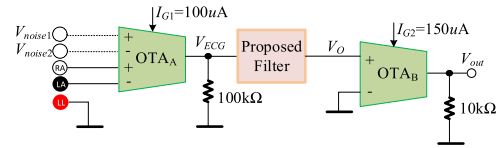

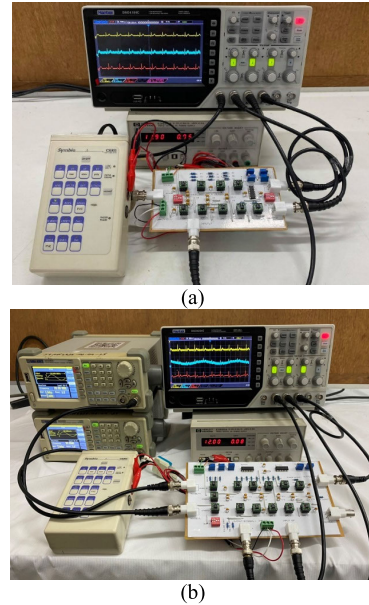**FIGURE 27.** Completed filter for 3-lead ECG signal experiment.

(a)

(b)

FIGURE 28. Experimental setup for ECG signal generator (a) LPF (b) BPF.

The frequency characteristic of the proposed MIOTA-based 5th-order LPF was verified by using Bode100 vector network analyzer (VNA) [37]. The cutoff frequency was regulated within 25-250Hz by regulating the bias currents (I_B) in the range 50-500μA as shown in Fig. 29. The variable gain of the proposed LPF is illustrated in Fig. 30. The gain can be adjusted up to 30dB by adjusting the bias current of OTA$_B$.
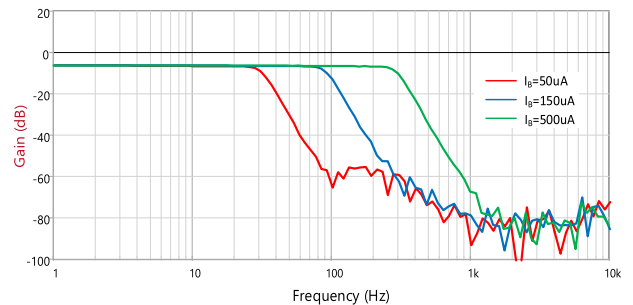

FIGURE 29. Frequency response of LPF (V_O) by tuning the bias current.

For the ECG application, the cutoff frequency of, 250Hz is required that is achieved for the bias current of 500μA. The in-band frequency has been tested by applying the sine wave signal of 20Hz and amplitude 210mVp-p at the input of the proposed LPF. Fig. 31 illustrates that the 3rd harmonic component output was appeared lower than the fundamental

TABLE 3. Comparison Between the Proposed Filters and Some Previous Works.

Parameter	This work		2018 [20]	2019 [22]	2009 [39]	2007 [40]	2018 [21]	2020 [41]
V_{DD}[V]	0.5	0.5	1	1	1	1	0.6	0.5
Vth [V]	0.5	0.5	0.5	0.5	0.5	0.7	0.7	0.5
Tech. [μm]	0.18		0.18	0.18	0.18	0.35	0.35	0.18
Order	5th LP	3rd BP	5th LP	5th LP	5th LP	3th BP	4th LP	4th LP
Method	ladder	ladder	ladder	ladder	ladder	ladder	cascade of two biquad	cascade of two biquad
Topology	single-end MIOTA-C	single-end OTA-C	fully OTA-C	fully OTA-C	fully OTA-C	single-end OTA-C	fully FVF	fully FSF
No. of device	5-OTA	6-OTA	6-OTA	6-OTA	11-OTA	8-OTA	–	–
f_c/BW [Hz]	250	250	50	250	250	670	101	200
DC gain [dB]	-6	-6	-6	-7	-10.5	0	-2.77	-5.6
Input-referred noise [μV$_{rms}$]	301	240	100	134	340	50	46.27	91.9
DR [dB]	57.6	60.4	49.9	61.2	50	49	47	48.5
Power [nW]	50	60	350	41	453	68	0.9	3.69
FOM	2.58E-14	3.77E-14	4.47E-12	2.85E-14	1.14E-12	1.26E-13	5.97E-15	8.66E-15
Area (mm^2)	0.036 (off chip cap.)	0.0435 (off chip cap.)	0.06 (off chip cap.)	0.24	0.13	0.234	0.168	0.074
Low voltage capability V_{TH}/V_{DD} (100%)	100	100	50	50	50	70	116.6	100
Obtained results	post-layout	post-layout	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.
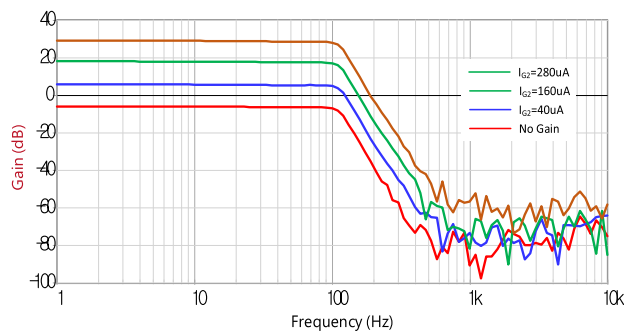
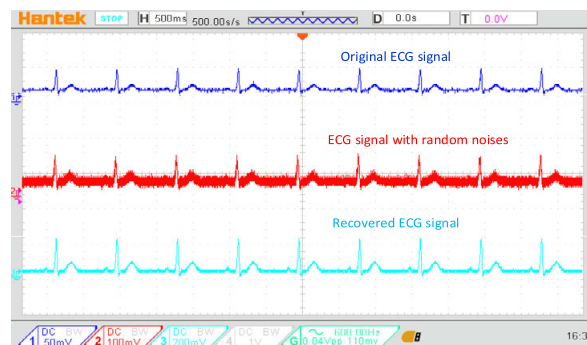**FIGURE 30.** Variable gain of LPF (V_{out}) obtained by the bias current of OTA$_B$.

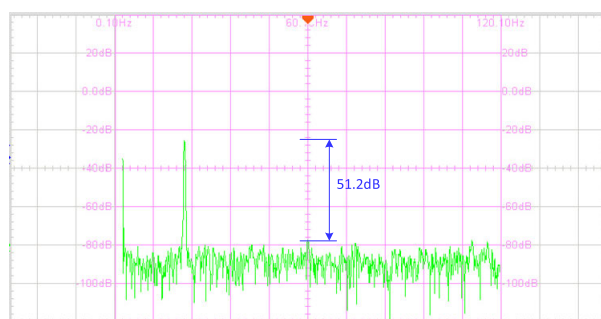**FIGURE 31.** Output spectrum of LPF based on 20Hz input.

FIGURE 32. Noisy ECG input signal and ECG output of LPF.

component by 51.2dB. The ECG signal from a generator with insertion noise was applied at the input of the proposed filter. The ECG output can be recovered without noise as shown in Fig. 32 agreed with the simulation result.

The frequency characteristic of the proposed MIOTA-based 3rd-order BPF was also verified by VNA. The frequency response tunability is provided by varying the bias current (I_B) from 10-100μA as shown in Fig. 33. The constant bandwidth has been carried out and illustrated by three bias current cases. The upper and lower cutoff frequencies were 5Hz and 3kHz for $I_B = 100\mu A$ (green line), 2Hz and 1kHz for $I_B = 30\mu A$ (blue line) and 0.5Hz and 300Hz for $I_B = 10\mu A$ (red line). It is noted for the red line that cannot be shown the lower cut-off frequency due to the VNA spanned is limited.

This proposed BPF allows independently adjust the upper and lower cutoff frequency by tuning the bias current of relevant OTA. The OTA$_2$, OTA$_3$ and OTA$_6$ control the lower cutoff frequency while OTA$_1$, OTA$_4$ and OTA$_5$ control the upper cutoff frequency. The independent tuning of the lower
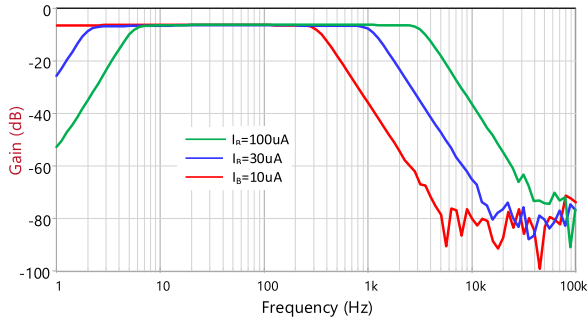
FIGURE 33. Frequency response of BPF with different bias current.

and upper cutoff frequency is illustrated in Figs. 34 and 35, respectively. The variable gain of the proposed BPF is illustrated in Fig. 36 which can be adjusted up to 30dB by regulating the bias current of OTA_B.
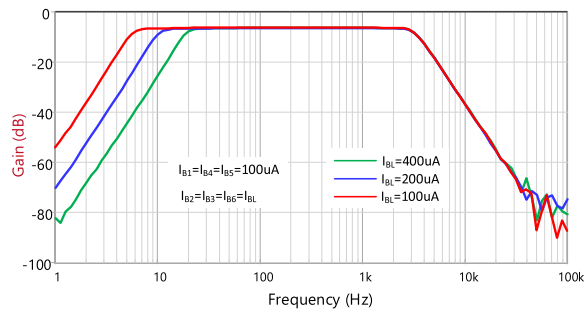

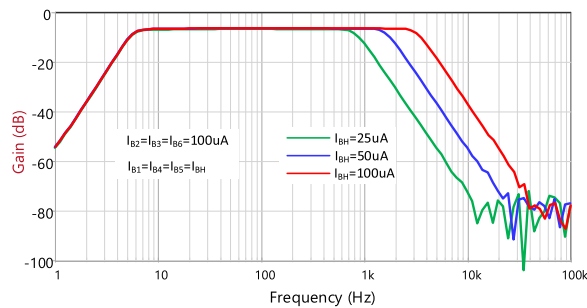**FIGURE 34.** Lower cutoff frequency of BPF tuning by the bias current.

FIGURE 35. Upper cutoff frequency of BPF tuning by the bias current.
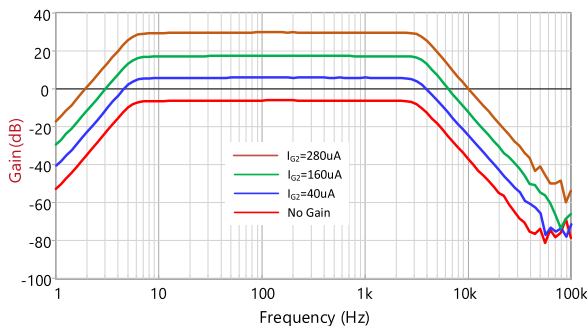

FIGURE 36. Variable gain of the proposed BPF tuning by the bias current.

For the ECG application with motion artifact reduction, the bandwidth of the BPF at 0.5-250Hz required that the bias current $10\mu A$ has been assigned. The in-band frequency

has been tested by applying the sine wave signal of 20Hz and amplitude of 210mVp-p at input of proposed BPF. Fig. 37 illustrates that the 2nd and 3rd harmonic components were lower than the fundamental component by 45.6 and 46.4dB, respectively.
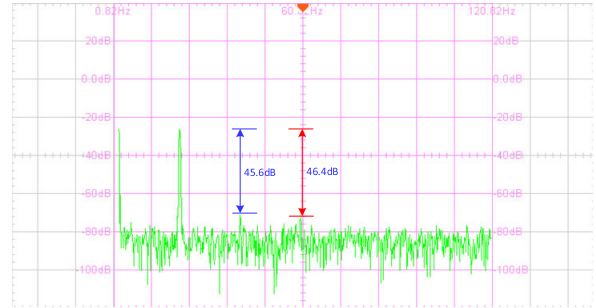

FIGURE 37. Output spectrum of BPF based on 20Hz input.
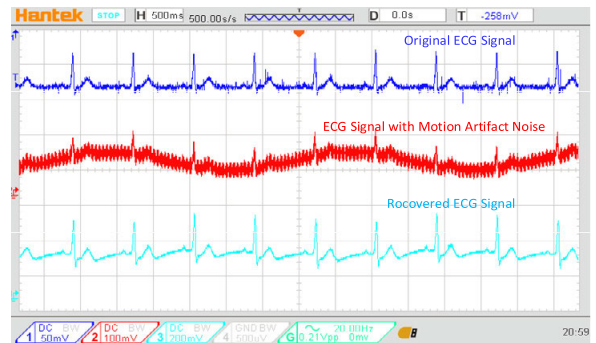

FIGURE 38. Noisy ECG input signal and ECG output of BPF.

The ECG signal from the generator with random noise and motion artifact noise (300mHz) was applied at the proposed BPF filter input. The clean ECG output can be recovered without motion artifact and random noises, as shown in Fig. 38, agreed with the simulation result.

Finally, it is worth mentioning that although the experimental results were obtained by commercially available OTA using a different power supply and power consumption but the design concept, the simplified structure, tunability, and actual application are confirmed consistent with the simulation results. Furthermore, the proposed MIOTA has two differential inputs (constructed by two commercially OTAs); hence the advantage of the MIOTA in terms of a reduced number of active elements and power consumption is evident.

VI. CONCLUSION
This paper presents a 5th-order Chebyshev low-pass and a 3rd order band-pass filters for ECG signal processing. The filters employ an innovative CMOS structure of OTA that exploits the bulk-driven, the self-cascode and the multiple-input to achieve enhanced linearity under 0.5V voltage supply. The simulation results including MC and PVT confirm the robustness of the circuit. The circuit functionality is also confirmed by commercially available OTA LT1228 and the experimental results agree with theory. The proposed filter can efficiently reduce the random noise and motion artifact noise in ECG.

The filter circuits offer attractive FoM and DR compared with most related published works.

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