RESEARCH ARTICLE

0.5 V Universal Filter and Quadrature Oscillator Based on Multiple-Input DDTA

MONTREE KUMNGERN[1], **FABIAN KHATEB**[2,3,4], **AND TOMASZ KULEJ**[5]

[1]Department of Telecommunications Engineering, School of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand
[2]Department of Microelectronics, Brno University of Technology, 601 90 Brno, Czech Republic
[3]Department of Electrical Engineering, Brno University of Defence, 662 10 Brno, Czech Republic
[4]Faculty of Biomedical Engineering, Czech Technical University in Prague, 166 36 Prague, Czech Republic
[5]Department of Electrical Engineering, Czestochowa University of Technology, 42-201 Czestochowa, Poland

Corresponding author: Montree Kumngern (montree.ku@kmitl.ac.th)

ABSTRACT This paper presents a universal voltage-mode filter and quadrature oscillator based on low-voltage multiple-input differential difference transconductance amplifier (MI-DDTA). Unlike the previous published DDTAs, that utilize the bulk-driven (BD) multiple-input MOS transistor technique (MI-MOST) in the differential pair of the first stage only, the proposed DDTA, for the first time, utilize the BD MI-MOST in the second stage of the DDTA. This results in capability of providing more arithmetic operations without additional current branches or power dissipation. Hence, simplify the topology of the filter and oscillator applications, by decreasing the count of active blocks. The voltage-mode filter offers high-input and low-output impedances, and both non-inverting and inverting versions of five types of transfer functions, namely low-pass, high-pass, band-pass, band-stop, and all-pass characteristics. The oscillator offers three-phase of quadrature signals, and orthogonal control of the condition and frequency of oscillations. The circuit was designed in Cadence environment using 180 nm CMOS TSMC technology. The voltage supply is 0.5 V and the power consumption of the filter is 472 nW. The simulation results are in accordance with theory and confirm the performance of the proposed circuit.

INDEX TERMS Differential difference transconductance amplifier, multiple-input MOS transistor technique, universal filter, quadrature oscillator.

I. INTRODUCTION

The differential difference amplifier (DDA) is a versatile building block that was proposed as a circuit alternative for the conventional operational amplifier (op-amp) [1]. Thanks to the increased number of inputs, the DDA can realize the operations of addition and extraction of input voltages without the need for passive elements [2]. When operating with a negative feedback loop, and doubled output stage, the DDA can be used for the realization of the differential difference current conveyor (DDCC) [3]. Unfortunately, DDCC does not provide an electronic tuning capability; hence, DDCC-based circuits usually require passive resistors [4], [5], [6], [7], [8], [9], [10].

The operational transconductance amplifier (TA) is a circuit implementation of a voltage-controlled current source. This is another building block that can be used for synthesis of analog circuits. The TA is a simple one-stage amplifier, without high-impedance internal nodes. Its transfer characteristics are characterized mainly by its transconductance (g_m), which can easily be tuned with external current (I_{set}). The TA-based circuits are most often realized without passive resistors, and their characteristics can easily be tuned by means of I_{set} [11].

To combine the advantages of DDA and TA into a single device, the new active blocks such as the differential difference current conveyor transconductance amplifier (DDCCTA) [12] and the differential difference transconductance amplifier (DDTA) [13], [14] were introduced. These devices offer an addition and subtraction of input voltages, with the result available at zero-impedance output, followed by an additional transconductance stage.

The associate editor coordinating the review of this manuscript and approving it for publication was Xi Zhu.
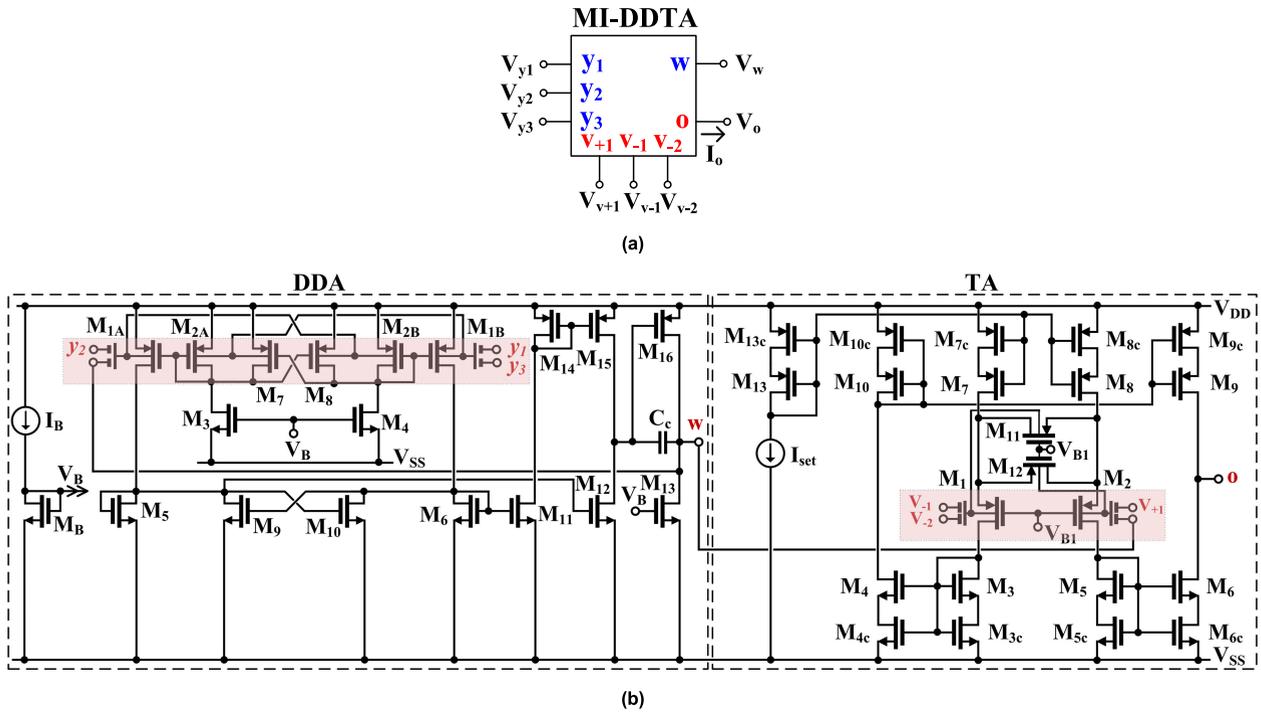
FIGURE 1. The MI-DDTA: electrical symbol (a) and the proposed CMOS structure (b).

The DDCCTAs and DDTAs are often used to implement quadrature oscillators [15], [16], [17] and universal filters [18], [19], [20], [21], [22], [23], [24].

Nowadays, low-voltage and low-power active filters have received considerable attention because they can be applied in biomedical and biosensor systems. The analog filters are used to select the required frequency range (in case of the band-pass filters) and to eliminate the out-of-band noise (in case of the low-pass filters). There are many low-voltage and low-power analog filters [21], [22], [23], [24], [25], [26], [27], [28], as well as signal generators [29], [30], [31], [32] available in the literature. The universal filters and oscillators based on low-voltage and low-power DDTAs have been proposed in [21] and [22]. The circuit in [21] employs three DDTAs and uses a 0.5 V supply, while the circuit in [22] employs two DDTAs and uses a 0.3 V supply voltage.

In this work a new universal voltage-mode filter and quadrature oscillator employing two low-voltage multiple-input DDTAs and two grounded capacitors is proposed. It will be shown that thanks to the MI-DDTAs many filtering responses can be obtained. Moreover, the proposed filter offers several advantages such as high-input and low-output impedance which is desirable in voltage-mode circuits, providing both non-inverting and inverting types of five basic transfer functions, namely low-pass (LPF), high-pass (HPF), band-pass (BPF), band-stop (BSF), and all-pass (APF) responses. The structure uses only grounded capacitors, which is suitable for integrated circuit implementations. The proposed filter can be modified to work as a quadrature

oscillator with orthogonal control of the condition and the frequency of oscillation.

II. CIRCUIT DESCRIPTIONS
A. PROPOSED MI-DDTA
The symbol of the MI-DDTA is shown in Fig. 1 (a). The properties of this MI-DDTA are similar to the previous DDTAs [21], [22], [23], [24], except the input terminals of the transconductance amplifier stage. Unlike the conventional solutions, in the proposed version the multiple-input inverting and non-inverting terminals of the transconductance amplifier are available, thus creating a more versatile active element that offers more arithmetic operations that simplify circuit structures of many applications. It is worth noting that the advantages of using multiple-input transconductors in reducing the number of components in OTA-C filters design was confirmed in the literature [39], [40]. It was confirmed that the multiple-input OTA can reduce the number of components, silicon area, and power dissipation by approximately factor k, where k is the number of OTA inputs [39].

In ideal case the main characteristics of the proposed MI-DDTA are given by

$$\left.\begin{array}{l} V_w = V_{y1} - V_{y2} + V_{y3} \\ I_o = g_m \left(V_w + V_{v+1} - V_{v-1} - V_{v-2} \right) \end{array}\right\} \quad (1)$$

The CMOS structure of the proposed MI-DDTA is shown in Fig. 1 (b). The circuit operates in subthreshold region and can be seen as a modification of the DDTA presented in [23]. It consists of a differential difference amplifier (DDA) followed by transconductance amplifier (TA). The DDA

employs the bulk-driven multiple-input MOS transistor as a differential pair M_{1A}, M_{2A}, M_{1B}, M_{2B} [23]. The symbol and the CMOS realization of the BD MI-MOST is shown in Fig. 2.
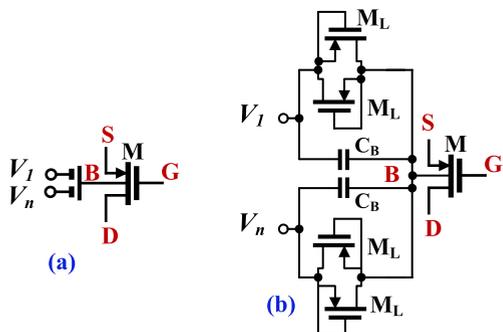
FIGURE 2. The BD MI-MOST: symbol (a) and the implementation (b).

The multiple-input are simply obtained by a parallel connection of capacitors C_B with high resistance anti-parallel connection of two minimum-size transistors M_L. The MI-MOST technique was experimental verified in [33], [34], [35], and [36]. Since the input capacitive divider decreases the voltage gain, a partial positive feedback (PPF) technique was applied. Transistors M_7, M_8 and M_9, M_{10} form two PPF circuits that generate negative resistances at gate/drain nodes of the diode-connected transistors M_{2AB} and M_5/M_6, respectively. Note, that in order to maintain the circuit stability, the transconductances of the PPF transistors should not exceed the transconductances of the corresponding diode-connected transistors, also in the presence of transistor mismatch and process, supply voltage, temperature (PVT) variations. Moreover, as the difference between the transconductances of the transistors in PPF circuits and the transconductances of the diode connected transistors is decreasing, then the circuit sensitivity to transistor mismatch is increasing, which can lead to increased variations of the gain bandwidth product (GBP), phase margin (PM), etc. As it was shown in [23], application of two PPF circuits with larger difference of transconductances can provide the same improvement of the voltage gain, with smaller overall sensitivity to transistor mismatch. Overall, the first stage of the proposed DDTA can be seen as a two-stage OTA, with MI differential stage at the input and 100% negative feedback, between output and one of the inputs. The capacitor C_C is used for frequency compensation.

Compared to [23] the main modification is related to the TA where the bulk-driven multiple-input MOS transistor is also used in the differential pair M_1, M_2. This modification enables more arithmetic operations without additional current branches or power dissipation. The TA also employs the source degeneration technique M_{11}, M_{12} to increase the linear range of the TA. The overall structure can be seen as a current mirror TA, where the current mirrors M_3-M_4, M_5-M_6 and M_9-M_{10} are composed of self-cascode transistors to improve the overall voltage gain of the circuit.

The small-signal transconductance of the TA is given by [33]:

$$G_m = \beta_i \eta \cdot \frac{4m}{4m+1} \cdot \frac{I_{set}}{n_p U_T} \qquad (2)$$

where $\eta = g_{mb1,2}/g_{m1,2}$ at the operating point, $\beta \approx 1/n$ where n is the number of differential inputs of the pair (here n = 2), n_p is the subthreshold slope factor and U_T is the thermal potential. The coefficient $m = (W/L)_{11,12}/(W/L)_{1,2}$. For optimum linearity $m = 0.5$ [33]. Note the circuit transconductance can be easily tuned with I_{set}.

Thanks to the BD MI-MOST and the source degeneration, the TA enjoys good linearity with nearly rail-to-rail input voltage range. Note, that the input noise of the MI-TA will be increased due to the lower transconductance, being a result of an input capacitive divider combined with a BD technique. However, the input range is extended in the same proportion, and hence, the dynamic range will not be affected [33]. Further improvement in circuit's performance could be achieved by employing the multiple-input bulk-driven quasi-floating-gate MOS transistor, where the MI-MOST is driven simultaneously from its gate and bulk terminal [35]. This results in increased total transconductance and reduced input noise, however at the cost of increased chip area [36].

It worth mentioning that although the standalone TA was firstly presented and experimentally verified in [33], this is the first time where it is used as a part of the DDTA in order to increase its performance and its arithmetic operation.

B. ANALOG FILTER USING MI-DDTAS

The proposed analog filter using MI-DDTAs is shown in Fig. 3. The circuit employs two MI-DDTAs and two grounded capacitors. It should be noted that the inputs V_{+in1}, V_{-in1}, V_{+in2}, V_{-in2}, V_{+in3}, and V_{-in3} are fed to the high impedance terminals of DDTAs while the outputs V_{o1} and V_{o2} are the low-impedance outputs W of the MI-DDTAs. Thus, a single input signal can be fed to variant input terminals whereas the outputs can be connected directly to the loads, without buffer circuits. Note that since the circuit offers inverting input terminals, the inverting-type input signal requirement is absent. The use of inverting-type input signal means that additional circuit is required to convert the conventional positive signal to negative (i.e., from function generator).
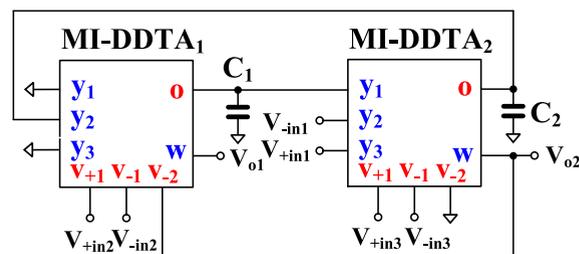
FIGURE 3. The Proposed analog filter using MI-DDTAs.

Using (1) and nodal analysis, the output voltages of the filter in Fig. 3 can be expressed by

$$V_{o1} = \frac{\left\{\begin{array}{l} sC_1 g_{m2}\left(V_{-in1}-V_{+in1}\right)+g_{m1}g_{m2}\left(V_{-in2}-V_{+in2}\right) \\ +\left(sC_1 g_{m2}+g_{m1}g_{m2}\right)\left(V_{-in3}-V_{+in3}\right)\end{array}\right\}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1}g_{m2}}$$

(3)

$$V_{o2} = \frac{\left\{\begin{array}{l} s^2 C_1 C_2\left(V_{+in1}-V_{-in1}\right)+sC_2 g_{m1}\left(V_{-in2}-V_{+in2}\right) \\ +g_{m1}g_{m2}\left(V_{-in3}-V_{+in3}\right)\end{array}\right\}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1}g_{m2}}$$

(4)

The filtering functions can be obtained by appropriately selecting the output terminals and appropriately applying the input signals as shown in Table 1.

TABLE 1. Obtaining variant filtering functions of the analog filter.

Filtering Function		Input	Output
LP	Non-inverting	V_{-in2}	V_{o1}
	Inverting	V_{+in2}	V_{o1}
	Non-inverting	V_{-in3} & V_{+in1}	V_{o1}
	inverting	V_{+in3} & V_{-in1}	V_{o1}
	Non-inverting	V_{-in3}	V_{o2}
	inverting	V_{+in3}	V_{o2}
BP	Non-inverting	V_{-in1}	V_{o1}
	Inverting	V_{+in1}	V_{o1}
	Non-inverting	V_{-in3} & V_{+in2}	V_{o1}
	Inverting	V_{+in3} & V_{-in2}	V_{o1}
	Non-inverting	V_{+in2}	V_{o2}
	Inverting	V_{-in1}	V_{o2}
HP	Non-inverting	V_{+in1}	V_{o2}
	Inverting	V_{-in1}	V_{o2}
BS	Non-inverting	V_{+in1} & V_{-in3}	V_{o2}
	Inverting	V_{-in1} & V_{+in3}	V_{o2}
AP	Non-inverting	V_{+in1} & V_{-in2} & V_{-in3}	V_{o2}
	Inverting	V_{-in1} & V_{+in2} & V_{+in3}	V_{o2}

The natural frequency (ω_o) and the quality factor (Q) are given by

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}}$$

(5)

$$Q = \sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}}$$

(6)

The parameter ω_o can be controlled by varying $g_{m1} = g_{m2}$ and keeping C_1 and C_2 to be constant whereas the parameter Q can be determined by the ratio C_1/C_2 while maintaining g_{m2}/g_{m1} to be constant. It should be noted that the parameter ω_o can also be controlled electronically.

The proposed analog filter can be modified to work as a quadrature oscillator as shown Fig. 4. The transfer function V_{o1}/V_{-in1} of the band-pass filter of Fig. 3 is used and it can be expressed by

$$\frac{V_{o1}}{V_{-in1}} = \frac{sC_1 g_{m2}}{s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1}g_{m2}}$$

(7)
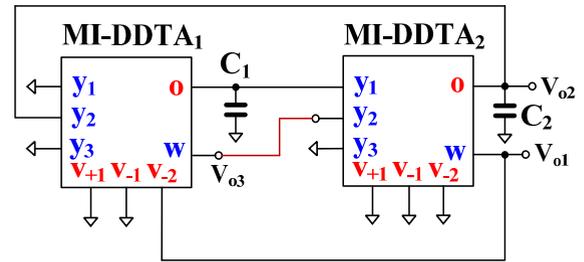
FIGURE 4. Modified quadrature oscillator using MI-DDTAs.

Letting $V_{o1}/V_{-in1} = 1$ (V_{o1} and V_{-in1} are connected), the characteristic equation of the oscillator can be given by

$$s^2 C_1 C_2 + s\left(C_2 g_{m1} - C_1 g_{m2}\right) + g_{m1}g_{m2} = 0$$

(8)

Letting $g_{m1} = g_{m2}$, the condition of oscillation is

$$C_2 = C_1$$

(9)

The frequency of oscillation is

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}}$$

(10)

The frequency of oscillation can be controlled electronically by g_m ($g_m = g_{m1} = g_{m2}$) while the condition of oscillation can be controlled by C_1 and/or C_2. Therefore, the frequency and condition of oscillation can be orthogonally controlled.

From Fig. 4, the transconductance amplifier of DDTA2 (g_{m2}) along with C_2 form a lossless integrator and its transfer function can be expressed as

$$\frac{V_{o2}}{V_{o1}} = \frac{g_{m2}}{sC_2}$$

(11)

Thus, the magnitude and phase difference ($\emptyset$) between V_{o1} and V_{o2} of this transfer function at oscillating frequency ($\omega = \omega_o$) are respectively $|g_{m2}/C_2|$ and $90°$. From Fig. 4, the output V_{o2} and V_{o3} are out of phase, thus the phase difference between V_{o1} and V_{o3} is $-90°$.

III. NONIDEALITIES ANALYSIS

To consider the non-ideal effect of a MI-DDTA, by taking the non-idealities properties of the DDTAs into account, the characteristics of the MI-DDTA can be rewritten as

$$\left.\begin{array}{l} V_w = \beta_{k1} V_{y1} - \beta_{k2} V_{y2} + \beta_{k3} V_{y3} \\ I_o = g_{mnk}\left(V_w + V_{v+1} - V_{v-1} - V_{v-2}\right)\end{array}\right\}$$

(12)

where β_{k1} is the voltage gain from V_{y1} to V_w of k-th DDTA, β_{k2} is the voltage gain from V_{y2} to V_w of k-th DDTA, β_{k3} is the voltage gain from V_{y3} to V_w of k-th DDTA, g_{mnk} is the non-ideal transconductance gain of k-th DDTA. The voltage gains $\beta_{k1}, \beta_{k2}, \beta_{k3}$ are unity for ideal case.

The non-ideal transconductance g_{mnk} of k-th DDTA can be expressed by [37]

$$g_{mnk}(s) \cong g_{mk}\left(1 - \mu_k s\right)$$

(13)

It is the frequency dependence of transconductance that usually considered around the operation frequency ω_o [38],

where $\mu_k = 1/\omega_{gmk}$, ω_{gmk} denotes the first pole of k-th transconductance.

Using (12), the output voltages of the circuit in Fig. 3 become

$$
V_{o1} = \frac{\left\{\begin{array}{c} sC_1 g_{m2}\left(\beta_{22}V_{-in1} - \beta_{23}V_{+in1}\right) \\ +g_{m1}g_{m2}\beta_{12}\beta_{21}\left(V_{-in2} - V_{+in2}\right) \\ +\left(sC_1 g_{m2}\beta_{12} + g_{m1}g_{m2}\beta_{12}\beta_{21}\right)\left(V_{-in3} - V_{+in3}\right) \end{array}\right\}}{s^2 C_1 C_2 + sC_2 g_{m1}\beta_{21} + g_{m1}g_{m2}\beta_{12}\beta_{21}}
$$
(14)

$$
V_{o2} = \frac{\left\{\begin{array}{c} s^2 C_1 C_2\left(\beta_{23}V_{+in1} - \beta_{22}V_{-in1}\right) \\ +sC_2 g_{m1}\beta_{12}\left(V_{-in2} - V_{+in2}\right) \\ +g_{m1}g_{m2}\beta_{12}\beta_{21}\left(V_{-in3} - V_{+in3}\right) \end{array}\right\}}{s^2 C_1 C_2 + sC_2 g_{m1}\beta_{21} + g_{m1}g_{m2}\beta_{12}\beta_{21}}
$$
(15)

Using (13), the denominator of (14)-(15) can be modified as

$$
s^2 C_1 C_2 \left(1 - \frac{C_2 g_{m1}\beta_{21} - g_{m1}g_{m2}\beta_{12}\beta_{21}\mu_1\mu_2}{C_1 C_2}\right)
$$
$$
+ sC_2 g_{m1}\beta_{21}\left(1 - \frac{g_{m1}g_{m2}\beta_{12}\beta_{21}\left(\mu_1 + \mu_2\right)}{C_1 C_2}\right)
$$
$$
+ g_{m1}g_{m2}\beta_{12}\beta_{21}
$$
(16)

The parasitic effects from the transconductance amplifiers can be made negligible by satisfying the following condition

$$
\left.\begin{array}{c} \dfrac{C_2 g_{m1}\beta_{21} - g_{m1}g_{m2}\beta_{12}\beta_{21}\mu_1\mu_2}{C_1 C_2} \ll 1 \\[2mm] \dfrac{g_{m1}g_{m2}\beta_{12}\beta_{21}\left(\mu_1 + \mu_2\right)}{C_1 C_2} \ll 1 \end{array}\right\}
$$
(17)

The natural frequency (ω_o) and the quality factor (Q) can be modified as

$$
\omega_o = \sqrt{\frac{g_{mn1}g_{mn2}}{C_1 C_2}\beta_{12}\beta_{21}}
$$
(18)

$$
Q = \sqrt{\frac{C_1 g_{mn2}}{C_2 g_{mn1}}\frac{\beta_{12}}{\beta_{21}}}
$$
(19)

Eq. (7) can be rewritten as

$$
\frac{V_{o1}}{V_{-in1}} = \frac{sC_1 g_{m2}\beta_{22}}{s^2 C_1 C_2 + sC_2 g_{m1}\beta_{21} + g_{m1}g_{m2}\beta_{12}\beta_{21}}
$$
(20)

The characteristic equation of oscillator can be modified as

$$
s^2 C_1 C_2 + s\left(C_2 g_{m1}\beta_{21} - C_1 g_{m2}\beta_{22}\right) + g_{m1}g_{m2}\beta_{12}\beta_{21} = 0
$$
(21)

Letting $g_{m1} = g_{m2}$, the modification of the condition of oscillation is

$$
C_2\beta_{21} = C_1\beta_{22}
$$
(22)

The frequency of oscillation become

$$
\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}\beta_{12}\beta_{21}}
$$
(23)

The error of voltage gains of MI-DDTAs will affect the frequency of oscillation of the oscillator whereas the effect on the condition of oscillation is relatively weak because voltages β_{21} and β_{22} can be compensated.

IV. SIMULATION RESULTS

The circuit was designed in Cadence environment using the 180 nm TSMC CMOS technology. The voltage supply was 0.5 V ($\pm$0.25V for the purpose of simulation) and the bias current for the MI-DDA was set to 40 nA and the nominal value of the setting current for the TA was set to $I_{set} = 10$ nA. The power consumption of the MI-DDTA was 236 nW. The transistors aspect ratio, capacitors value and bias voltage are included in Table 2.

To demonstrate the advantages of the TA, Fig. 5 shows the simulated results of the DC transfer characteristic of the used TA (a) that was firstly presented in [33] with the TA (b) presented in [23]. Here it is evident the high linearity offered by the TA based on MI-MOST and source degeneration.

TABLE 2. Transistor aspect ratio of the MI-DDTA.

DDA	W/L (μm/μm)	TA	W/L (μm/μm)
M_{1A}, M_{2A}, M_{1B}, M_{2B} M_{14}, M_{15}	16/3	M_1, M_2	2×15/1
M_3-M_8, M_{11}-M_{12}, M_B	8/3	M_3-M_6	2×10/1
M_9, M_{10}	4/3	M_{3c}-M_{6c}	10/1
M_{16}	6×16/3	M_7-M_{10}, M_{13}	2×15/1
M_{13}	6×8/3	M_{7c}-M_{10c}, M_{13c},M_{11}, M_{12}	15/1
M_L	5/4	M_L	5/4
MIM capacitor: C_B= 0.5 pF, C_c= 6 pF		V_B=-100mV	

(a)

(b)
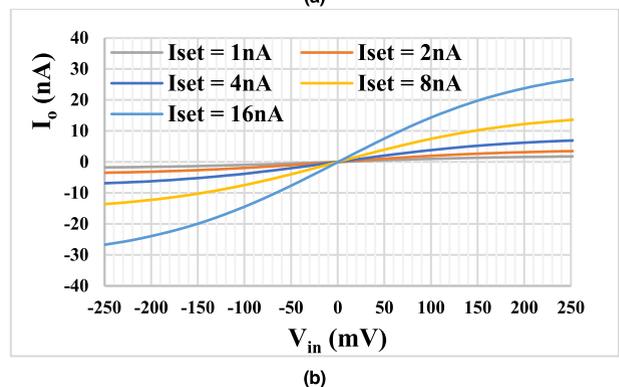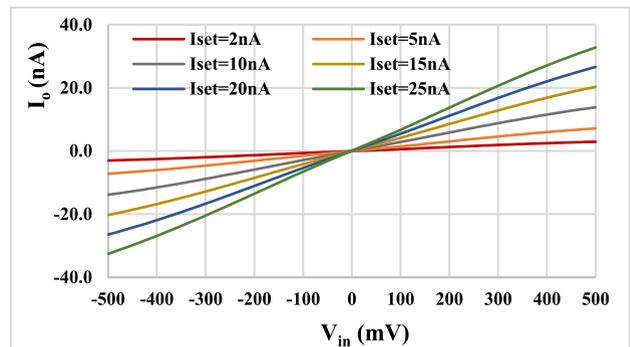
FIGURE 5. The DC transfer characteristic of the TA: [33] (a), and [23] (b).

The simulated frequency responses of the proposed filter are shown in Fig. 6. The values of $C_1 = C_2 = 15$ pF and the setting current $I_{set} = 10$ nA. The simulated cut-off frequency was 281 Hz and the calculated value was 286.6 Hz. The power consumption of the filter was 472 nW.
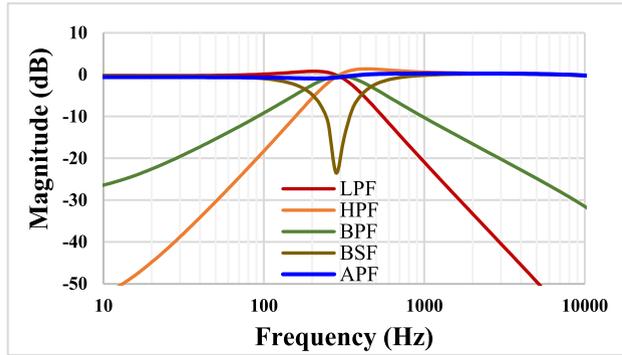
FIGURE 6. The frequency responses of the proposed filter.

Fig. 7 shows the tuning capability of the filter with $C_1 = C_2 = 15$ pF, the setting current was $I_{set} = 5$ nA, 10 nA and 20 nA and the cut off frequencies were 158.48 Hz, 281.83 Hz, 562.34 Hz, respectively. This figure confirm the wide tuning capability of the proposed filter for low frequency applications.

Figs. 8 and 9 show the simulation results of the LPF (a), HPF (b), BPF (c) and BSF (d) with 200 runs Monte Carlo (MC) analysis and process, voltage and temperature variation, respectively. The process corners were fast-fast, fast-slow, slow-fast and slow-slow, the voltage supply corners were in range $V_{DD} \pm 10\%$ and the temperature corners were $-10°C$ and $70°C$. Both figures confirm acceptable variation in these functions.

The transient response of the LPF and its spectrum are shown in Fig. 10. To the input terminal of the LPF was applied a sine wave signal of 200 mV$_{pp}$ @100 Hz. The Spurious Free Dynamic Range (SFDR) was -42.72 dB and the Total Harmonic Distortion (THD) was 0.82 %. The output noise characteristic of the LPF is shown in Fig. 11. The integrated noise was found 190 μV that results in dynamic range (DR) 51.4 dB.

By applying two tones test with 50mV amplitude at 281.83 Hz and at 291.83Hz, the third-order intermodulation distortion (IMD3) of the LPF was found -46 dB as shown in Fig. 12.

For the proposed oscillator in Fig. 4, the capacitor values were selected $C_1 = C_2 = 100$ pF. Fig. 13 shows the starting oscillation (a) the steady state (b) and the output spectrum (c), respectively. The frequency was 45 Hz and the second harmonic was around -40 dB below the fundamental. The simulated phase noise shows -68.5 dBc/Hz at 10 Hz offset from the center frequency.

Table 3 shows the performance comparison with previous universal filters. Compared with [21], [23], [27] the proposed filter has less count of active devices, compared with [22]
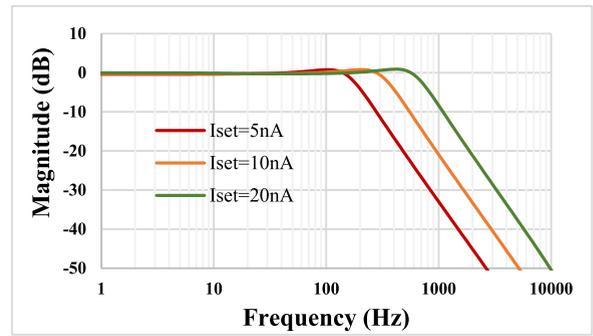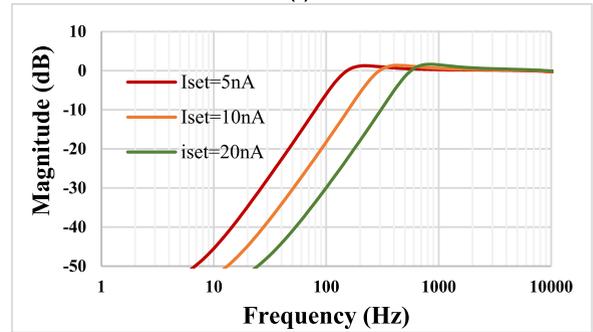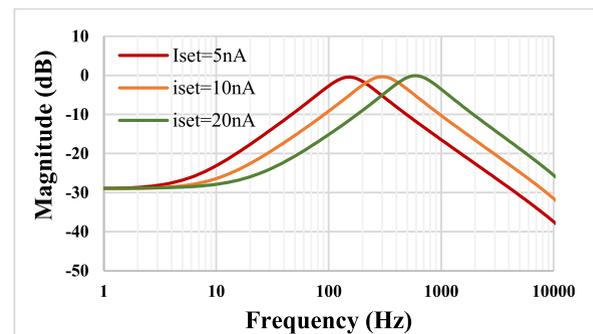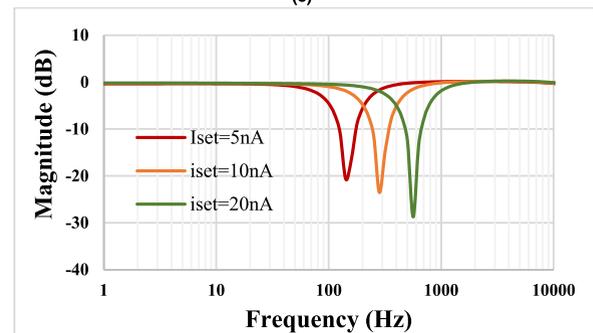
FIGURE 7. The tuning capability of the proposed filter: LPF (a), HPF (b), BPF (c) and BSF (d).

the proposed filter offers low output impedance and both non-inverting and inverting of five type filtering functions. Compared with [27], [28] the proposed filter is absent from minus-type input signal [27] and input voltage gain, i.e., 2V$_{in}$ [28].
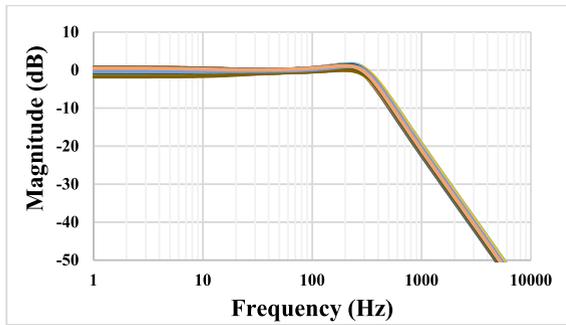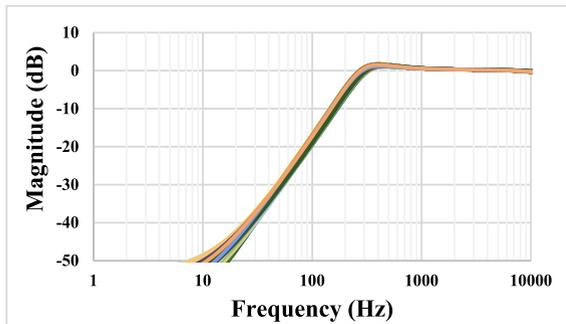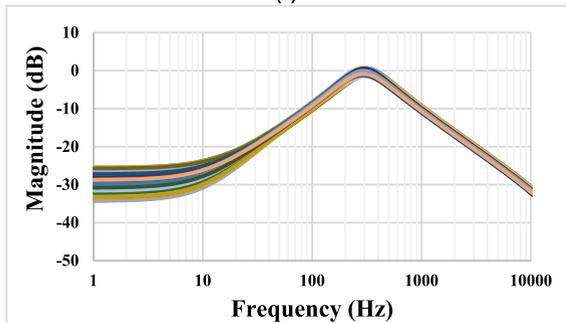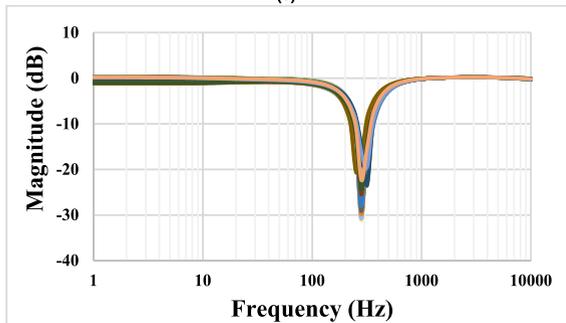
FIGURE 8. The 200 runs Monte Carlo analysis of the LPF (a), HPF (b), BPF (c) and BSF (d).

FIGURE 9. The PVT simulation of the LPF (a), HPF (b), BPF (c) and BSF (d).

It can be concluded that the proposed voltage-mode DDTA provides more arithmetic operation that can be served for minimum active/passive requirements of the proposed filter and oscillator. It should be noted that the multiple input of DDTA can offer many transfer functions of filter, both non-inverting and inverting filtering responses of LP, HP, BP, BS, and AP filters, and enables easy feedback connection for realizing filter or oscillator without additional passive

components. Please note that many transfer functions with minimum active elements can be possible by using MI-DDTA based circuit.

Compared with the conventional op-amp-based (or OTA-based) application, arithmetic operation (i.e. addition and subtraction) that usually required for realizing filter or oscillator, the single differential pair of these devices limit the applications such as applying the input signal or connecting

TABLE 3. Comparisons table with previous filters.

Features	Proposed	[21]	[22]	[23]	[27]	[28]
Active and passive elements	2 DDTA, 2 C	3 DDTA, 2 C, 1-R	2 DDTA, 2 C	3 DDTA, 2 C	8 OTA, 2 C	11 Inverter, 2-C
Realization	CMOS structure (0.18 μm)	CMOS structure (0.13 μm)	CMOS structure (0.13 μm)	CMOS structure (0.18 μm)	CMOS structure (0.18 μm)	CNTFET (0.32 μm)
Filter type	MIMO	MIMO	MIMO	MIMO	MIMO	MIMO
Number of filtering functions	18 (VM)	36 (VM)	22 (VM)	23 (VM)	20 (MM)	9 (CM, VM)
High-input and low-output impedance	Yes	No	No	No	No	No
Offering non-inverting and inverting filters	Yes	Yes	No	No	No	No
Electronic control of parameter ω_o	Yes	Yes	Yes	Yes	Yes	Yes
Offer universal filter and oscillator	Yes	Yes	Yes	No	No	No
Natural frequency (kHz)	0.281	0.2317	0.08147	0.254	5	1070
Total harmonic distortion (%)	0.8@200mV$_{pp}$	1.0@80 mV$_{pp}$	0.5@100 mV$_{pp}$	1.2@120 mV$_{pp}$	3@140 mV$_{pp}$ (LP)	-
Power supply voltages (V)	0.5	0.5	0.3	0.5	0.6	0.4
Dynamic range (dB)	51.4	53.27	-	49.7	53.2	-
Power consumption (μW)	0.472	0.831	0.715	0.616	5.77	0.447
FOM=P/(N*BW*DR) (pJ)	16.33	33.66	-	24.36	10.84	-
Verification of result	Sim	Sim/Exp	Sim	Sim	Sim	Sim

Note: MM = mixed-mode, CNTFET = carbon nanotube field-effect transistor, CM = current-mode.
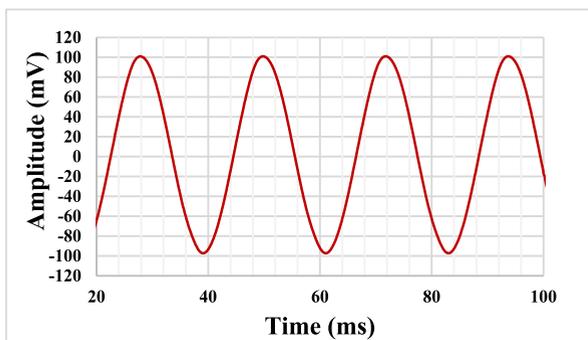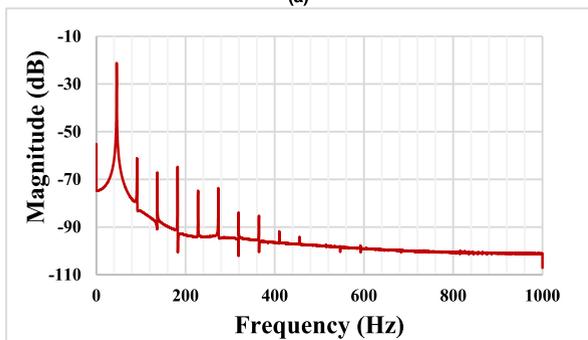
FIGURE 10. The transient response of the LPF (a) and its spectrum (b).

FIGURE 11. The output noise characteristic of the LPF.
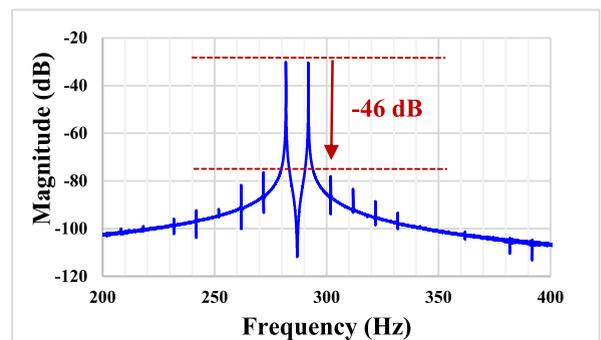
FIGURE 12. The output spectrum of the two tones test of the LPF.

the negative or positive feedback (in case oscillator). Thus, these op-amp-based (or OTA-based) addition and subtraction are usually required many passive resistors, which results in

complex realization and extra consumed chip area. This is evident compared with [22] that has equal active and passive components, the proposed filter can offer both non-inverting
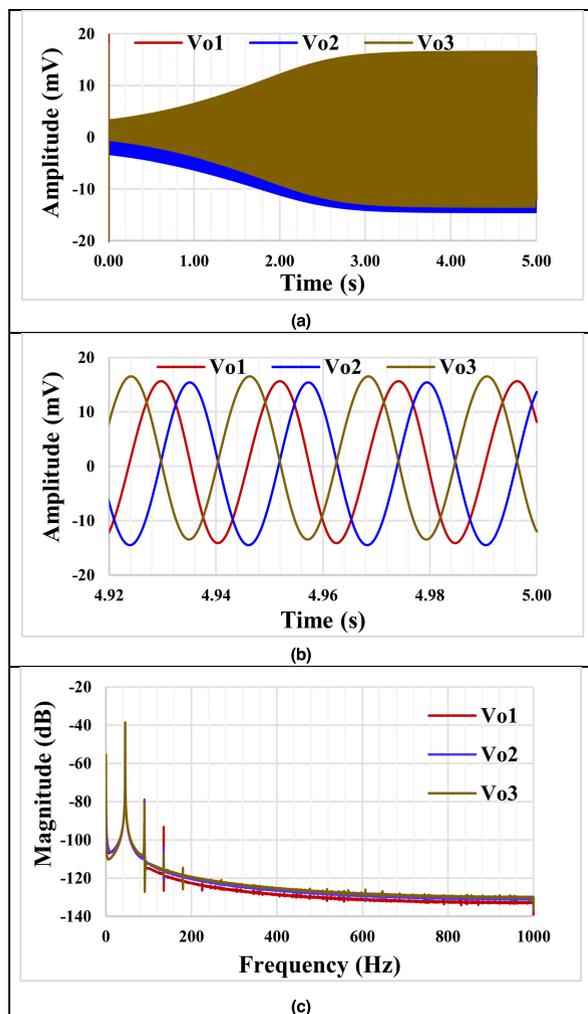
FIGURE 13. The starting oscillation (a) the steady state (b) and the output spectrum (c).

and inverting filtering responses of LP, HP, BP, BS, and AP filters, and low-output terminal which is ideal of VM circuits for applications.

V. CONCLUSION

This paper presents a low-voltage and low-power universal voltage-mode filter and quadrature oscillator using only two MI-DDTAs and two grounded capacitors. Unlike the previous presented DDTAs, where the MI-MOST forms only the differential pair of the DDA stage, in the presented DDTA this technique forms also the differential pair of the TA. This results in a simple CMOS structure that offers more arithmetic operation without increasing in current branches and power dissipation. The presented filter and oscillator applications were designed and verified in Cadence environment using 0.5 V supply voltage and 180 nm TSMC CMOS technology.

REFERENCES

[1] J. H. Huijsing, "Instrumentation amplifiers: A comparative study on behalf of monolithic integration," *IEEE Trans. Instrum. Meas.*, vol. IM-25, no. 3, pp. 227–231, Sep. 1976, doi: 10.1109/TIM.1976.6312351.

[2] E. Sackinger and W. Guggenbuhl, "A versatile building block: The CMOS differential difference amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 2, pp. 287–294, Apr. 1987, doi: 10.1109/JSSC.1987.1052715.

[3] W. Chiu, S. I. Liu, H. W. Tsao, and J. J. Chen, "CMOS differential difference current conveyors and their applications," *IEE Proc. Circuits, Devices Syst.*, vol. 143, no. 2, pp. 91–96, Apr. 1996, doi: 10.1049/ip-cds:19960223.

[4] M. Kumngern and K. Dejhan, "DDCC-based quadrature oscillator with grounded capacitors and resistors," *Active Passive Electron. Compon.*, vol. 2009, Jan. 2009, Art. no. 987304, doi: 10.1155/2009/987304.

[5] S. K. Mishra, M. Gupta, and D. K. Upadhyay, "Design and implementation of DDCC-based fractional-order oscillator," *Int. J. Electron.*, vol. 106, no. 4, pp. 581–598, Apr. 2019, doi: 10.1080/00207217.2018.1545260.

[6] A. Abaci and E. Yuce, "Single DDCC based new immittance function simulators employing only grounded passive elements and their applications," *Microelectron. J.*, vol. 83, pp. 94–103, Jan. 2019, doi: 10.1016/j.mejo.2018.11.014.

[7] M. Kumngern, F. Khateb, and T. Kulej, "Extremely low-voltage low-power differential difference current conveyor using multiple-input bulk-driven technique," *AEU Int. J. Electron. Commun.*, vol. 123, Aug. 2020, Art. no. 153310, doi: 10.1016/j.aeue.2020.153310.

[8] T. Unuk and E. Yuce, "Supplementary DDCC+ based universal filter with grounded passive elements," *AEU Int. J. Electron. Commun.*, vol. 132, Apr. 2021, Art. no. 153652.

[9] C. K. Choubey and S. K. Paul, "Nth order voltage-mode universal filter employing only plus type differential difference current conveyor," *Anal. Integr. Circuits Signal Process.*, vol. 110, no. 1, pp. 197–210, Jan. 2022, doi: 10.1007/s10470-021-01967-z.

[10] K. Orman, A. Yesil, and Y. Babacan, "DDCC-based meminductor circuit with hard and smooth switching behaviors and its circuit implementation," *Microelectron. J.*, vol. 125, Jul. 2022, Art. no. 105462, doi: 10.1016/j.mejo.2022.105462.

[11] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits Devices Mag.*, vol. DM-1, no. 2, pp. 20–32, Mar. 1985, doi: 10.1109/MCD.1985.6311946.

[12] N. Pandey and S. K. Paul, "Differential difference current conveyor transconductance amplifier: A new analog building block for signal processing," *J. Electr. Comput. Eng.*, vol. 2011, pp. 1–10, Jan. 2011, doi: 10.1155/2011/361384.

[13] M. Kumngern, "DDTA and DDCCTA: New active elements for analog signal processing," in *Proc. IEEE Int. Conf. Electron. Des., Syst. Appl. (ICEDSA)*, Kuala Lumpur, Malaysia, Nov. 2012, pp. 141–145.

[14] M. Kumngern, "CMOS differential difference voltage follower transconductance amplifier," in *Proc. IEEE Int. Circuits Syst. Symp. (ICSyS)*, Langkawi, Malaysia, Sep. 2015, pp. 133–136, doi: 10.1109/CircuitsAndSystems.2015.7394080.

[15] M. Kumngern, A. Auttaput, and K. Dejhan, "DDCCTA-based quadrature oscillator," in *Proc. 11th Int. Conf. ICT Knowl. Eng.*, Nov. 2013, pp. 1–4, doi: 10.1109/ICTKE.2013.6756282.

[16] P. Phatsornsiri, P. Lamun, and M. Kumngern, "Mixed-mode quadrature oscillator using a single DDCCTA and grounded passive components," in *Proc. 7th Int. Conf. Inf. Technol. Electr. Eng. (ICITEE)*, Oct. 2015, pp. 500–503, doi: 10.1109/ICITEED.2015.7408998.

[17] M. Siripruchyanun, "A CMOS electronically controllable current-mode sinusoidal quadrature oscillator using single DDCCTA and grounded passive elements," in *Proc. 38th Int. Conf. Telecommun. Signal Process. (TSP)*, Jul. 2015, pp. 1–5, doi: 10.1109/TSP.2015.7296408.

[18] P. Rana and A. Ranjan, "Odd- and even-order electronically controlled wave active filter employing differential difference trans-conductance amplifier (DDTA)," *Int. J. Electron.*, vol. 108, no. 10, pp. 1623–1651, Oct. 2021.

[19] O. Channumsin and W. Tangsrirat, "Single-input four-output voltage-mode universal filter using single DDCCTA," *Microelectron. J.*, vol. 44, no. 12, pp. 1084–1091, Dec. 2013.

[20] H.-P. Chen and S.-F. Wang, "High-input impedance tunable DDCCTA-based voltage-mode universal filter with grounded capacitors and resistors," *AEU Int. J. Electron. Commun.*, vol. 70, no. 4, pp. 491–499, Apr. 2016.

[21] M. Kumngern, P. Suksaibul, F. Khateb, and T. Kulej, "Electronically tunable universal filter and quadrature oscillator using low-voltage differential difference transconductance amplifiers," *IEEE Access*, vol. 10, pp. 68965–68980, 2022, doi: 10.1109/ACCESS.2022.3186435.

[22] F. Khateb, M. Kumngern, T. Kulej, and D. Biolek, "0.3-volt rail-to-rail DDTA and its application in a universal filter and quadrature oscillator," *Sensors*, vol. 22, no. 7, p. 2655, Mar. 2022, doi: 10.3390/s22072655.

[23] F. Khateb, M. Kumngern, T. Kulej, and D. Biolek, "0.5 V differential difference transconductance amplifier and its application in voltage-mode universal filter," *IEEE Access*, vol. 10, pp. 43209–43220, 2022.

[24] M. Kumngern, P. Suksaibul, F. Khateb, and T. Kulej, "1.2 V differential difference transconductance amplifier and its application in mixed-mode universal filter," *Sensors*, vol. 22, no. 9, p. 3535, May 2022, doi: 10.3390/s22093535.

[25] W. Jaikla, F. Khateb, M. Kumngern, T. Kulej, R. K. Ranjan, and P. Suwanjan, "0.5 V fully differential universal filter based on multiple input OTAs," *IEEE Access*, vol. 8, pp. 187832–187839, 2020, doi: 10.1109/ACCESS.2020.3030239.

[26] A. Namdari and M. Dolatshahi, "A new ultra low-power, universal OTA-C filter in subthreshold region using bulk-drive technique," *AEU Int. J. Electron. Commun.*, vol. 82, pp. 458–466, Dec. 2017.

[27] A. Namdari and M. Dolatshahi, "Design of a low-voltage and low-power, reconfigurable universal OTA-C filter," *Anal. Integr. Circuits Signal Process.*, vol. 111, pp. 169–188, May 2022.

[28] S. M. A. Zanjani, M. Dousti, and M. Dolatshahi, "A new low-power, universal, multi-mode Gm-C filter in CNTFET technology," *Microelectron. J.*, vol. 90, pp. 342–352, Aug. 2019, doi: 10.1016/j.mejo.2019.01.003.

[29] W.-C. Lai, S.-L. Jang, H. C. Lee, and J.-W. Jhuang, "CMOS quadrature voltage controlled oscillator uses in measuring blood glucose applications," in *Proc. 9th Int. Congr. Image Signal Process., Biomed. Eng. Informat. (CISP-BMEI)*, Oct. 2016, pp. 1472–1475, doi: 10.1109/CISP-BMEI.2016.7852749.

[30] H. Hu, S. Gupta, and M. Schiavenato, "An 143 nW relaxation oscillator for ultra-low power biomedical systems," in *Proc. IEEE SENSORS*, Oct. 2016, pp. 1–3, doi: 10.1109/ICSENS.2016.7808755.

[31] O. Olabode, A. Ontronen, V. Unnikrishnan, M. Kosunen, and J. Ryynanen, "A VCO-based ADC with relaxation oscillator for biomedical applications," in *Proc. 25th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2018, pp. 861–864, doi: 10.1109/ICECS.2018.8617935.

[32] B. T. Anjanakumari, C. M. Bhoomika, A. A. Jugale, and M. R. Ahmed, "Memristor based relaxation oscillator for biomedical applications," in *Proc. 3rd Int. Conf. Trends Electron. Informat. (ICOEI)*, Apr. 2019, pp. 1–5, doi: 10.1109/ICOEI.2019.8862738.

[33] F. Khateb, T. Kulej, M. Akbari, and K.-T. Tang, "A 0.5-V multiple-input bulk-driven OTA in 0.18-μm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 11, pp. 1739–1747, Nov. 2022, doi: 10.1109/TVLSI.2022.3203148.

[34] F. Khateb, T. Kulej, M. Kumngern, and C. Psychalinos, "Multiple-input bulk-driven MOS transistor for low-voltage low-frequency applications," *Circuits, Syst., Signal Process.*, vol. 38, pp. 2829–2845, Jun. 2019, doi: 10.1007/s00034-018-0999-x.

[35] F. Khateb, T. Kulej, H. Veldandi, and W. Jaikla, "Multiple-input bulk-driven quasi-floating-gate MOS transistor for low-voltage low-power integrated circuits," *AEU Int. J. Electron. Commun.*, vol. 100, pp. 32–38, 2019, doi: 10.1016/j.aeue.2018.12.023.

[36] F. Khateb, T. Kulej, M. Kumngern, W. Jaikla, and R. K. Ranjan, "Comparative performance study of multiple-input bulk-driven and multiple-input bulk-driven quasi-floating-gate DDCCs," *AEU Int. J. Electron. Commun.*, vol. 108, p. 1928, Aug. 2019, doi: 10.1016/j.aeue.2019.06.003.

[37] T. Tsukutani, M. Higashimura, N. Takahashi, Y. Sumi, and Y. Fukui, "Versatile voltage-mode active-only biquad with lossless and lossy integrator loop," *Int. J. Electron.*, vol. 88, pp. 1093–1102, Oct. 2001.

[38] H. Pevarez-Lozano and E. Sanchez-Sinencio, "Minimum parasitic effects biquadratic OTA-C filter architectures," *Anal. Integr. Circuits Signal Process.*, vol. 1, no. 4, pp. 297–319, Dec. 1991, doi: 10.1007/BF00239678.

[39] A. Wyszynski and R. Schaumann, "Using multiple-input transconductors to reduce number of components in OTA-C filter design," *Electron. Lett.*, vol. 28, pp. 217–220, Jan. 1992, doi: 10.1049/el:19920135.

[40] V. Gopinathan, Y. P. Tsividis, K.-S. Tan, and R. K. Hester, "Design considerations for high-frequency continuous-time filters and implementation of an antialiasing filter for digital video," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1368–1378, Dec. 1990, doi: 10.1109/4.62164.

MONTREE KUMNGERN received the B.S.Ind.Ed. degree in electrical engineering from the King Mongkut's University of Technology Thonburi, Thailand, in 1998, and the M.Eng. and D.Eng. degrees in electrical engineering from the King Mongkut's Institute of Technology Ladkrabang, Thailand, in 2002 and 2006, respectively. In 2007, he worked as a Lecturer with the Department of Telecommunications Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang. From 2010 to 2017, he worked as an Assistant Professor. Currently, he is an Associate Professor. He has authored or coauthored over 200 publications in journals and proceedings of international conferences. His research interests include analog and digital integrated circuits, discrete-time analog filters, non-linear circuits, data converters, and ultra-low voltage building blocks for biomedical applications.

FABIAN KHATEB received the M.Sc. degree in electrical engineering and communication, the M.Sc. degree in business and management, the Ph.D. degree in electrical engineering and communication, and the Ph.D. degree in business and management from the Brno University of Technology, Czech Republic, in 2002, 2003, 2005, and 2007, respectively. He is currently a Professor with the Department of Microelectronics, Faculty of Electrical Engineering and Communication, Brno University of Technology, Department of Electrical Engineering, University of Defence, Brno, and Department of Information and Communication Technology in Medicine, Faculty of Biomedical Engineering, Czech Technical University in Prague. He holds five patents. He has authored or coauthored over 100 publications in journals and proceedings of international conferences. He has expertise in new principles of designing low-voltage low-power analog circuits, particularly biomedical applications. He is a member of the Editorial Boards of *Microelectronics Journal*, *Sensors*, *Electronics*, and *Journal of Low Power Electronics and Applications*. He is an Associate Editor of IEEE ACCESS, *Circuits, Systems and Signal Processing*, *IET Circuits, Devices and Systems*, and *International Journal of Electronics*. He was a Lead Guest Editor of the Special Issues on Low Voltage Integrated Circuits and Systems on *Circuits, Systems, and Signal Processing*, in 2017, *IET Circuits Devices and Systems*, in 2018, and *Microelectronics Journal*, in 2019. He was also a Guest Editor for the Special Issue on Current-Mode Circuits and Systems: Recent Advances, Design and Applications in the *International Journal of Electronics and Communications*, in 2017.

TOMASZ KULEJ received the M.Sc. and Ph.D. degrees from the Gdańsk University of Technology, Gdańsk, Poland, in 1990 and 1996, respectively. He was a Senior Design Analysis Engineer at the Polish branch of Chipworks Inc., Ottawa, Canada. He is currently an Associate Professor with the Department of Electrical Engineering, Częstochowa University of Technology, Poland, where he lectures on electronics fundamentals, analog circuits, and computer aided design. He has authored or coauthored over 90 publications in peer-reviewed journals and conferences. He holds three patents. His recent research interests include analog integrated circuits in CMOS technology, with anemphasis on low voltage and low power solutions. He serves as an Associate Editor for the *Circuits Systems and Signal Processing* and *IET Circuits Devices and Systems*. He was also a Guest Editor for the Special Issues on Low Voltage Integrated Circuits on *Circuits Systems and Signal Processing*, in 2017, *IET Circuits Devices and Systems*, in 2018, and *Microelectronics Journal*, in 2019.

● ● ●