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RESEARCH ARTICLE

Reconfigurable Voltage-Mode First-Order Multifunction Filter Employing Second-Generation Voltage Conveyor (VCII) With Complete Standard Functions and Electronically Controllable Modification

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ABSTRACT In this contribution, the realization of a first-order, two-input, single-output voltage-mode multifunction filter employing a second-generation voltage conveyor (VCII) is described. The proposed first-order versatile filter is extremely simple, composed of a single VCII and three passive devices. Because of its low output impedance, the output voltage node can be easily cascaded with other voltage-mode configurations without the requirement of any buffers. In the same circuit topology, the proposed first-order filter provides various filtering functions: inverting and non-inverting low-pass (LPF), inverting and non-inverting high-pass (HPF), as well as inverting and non-inverting all-pass (APF). The digital method allows the selection of output first-order filtering functions without the need for additional circuits such as inverting or double-gain amplifiers. Furthermore, the pass-band gain of the low-pass and high-pass responses can be adjusted by varying the resistance or capacitance values without influencing the pole frequency as well as the phase response. The influence of VCII's current/voltage gain errors and parasitic elements on filtering performance is also investigated. Moreover, the modification of the proposed lagging phase all-pass filter to achieve electronic controllability is also proposed by replacing the passive resistor with the operational transconductance amplifier (OTA). The 0.18μm TSMC CMOS structure of the VCII employed in the proposed filter operates in the subthreshold region and utilizes the bulk-driven technique (BD), enabling it to operate with 0.4V supply voltage and consuming 383 nW of power. The total harmonic distortion (THD) of the LPF with an applied input voltage V_{inpp} =300mV @ 50Hz is -49.5 dB. An application example as a quadrature sinusoidal oscillator realized from the proposed first-order allpass filter and lossless integrator is also included. The performance of the proposed reconfigurable voltage-mode first-order filter is simulated and experimentally tested using a commercially available AD844 IC-based VCII with ±5 V power supply.

INDEX TERMS First-order filter, second-generation voltage conveyor, low-voltage, low-power CMOS.

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I. INTRODUCTION

First-order filters are significant circuits in analog signal processing systems, for example, communications, sound

systems, medical systems, instrumentation, etc. They are also commonly employed as a sub-circuit in the design of higher-order analog filter topologies, single/quadrature sinusoidal oscillators, and multiphase sinusoidal oscillators [1], [2], [3], [4], [5], [6]. The low-pass and high-pass filters (LPF and HPF) are utilized in a variety of applications to separate desired signals from unwanted signals based on frequency. The all-pass filter (APF), however, serves a different purpose. While the output signal's magnitude is kept constant, the APF is utilized to alter the output signal's phase. An all-pass filter is another name for the phase shifter. There are two kinds of phase shifters: lagging and leading phase configurations. For the analog first-order filtering system, the phase shift can be changed from low frequency to high frequency by 0 to -180 degrees (lagging phase) and by 180 to 0 degrees (leading phase).

The second-generation current conveyor (CCII) is an active building block (ABB) that is used to design both current and voltage mode circuits, whereas the CCII-based current-mode circuits give many advantages such as wide bandwidth, greater linearity, a wider dynamic range, simple circuitry, and low power consumption [7]. However, it is well known that it does not have a low-impedance voltage output terminal. So, CCII can't be used in some applications that need a voltage-based output signal without an external voltage buffer. It is obvious that a new active building block with low-impedance voltage output capability is useful for many analog signal processing applications like analog filters, inverse filters, and sinusoidal oscillators, etc. Second-generation voltage conveyor (VCII) is a versatile block [8], [9], [10], which is the dual of CCII, and it has been used for applications [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31] requiring low-impedance voltage output. This new ABB has an advantage over CCII and previous current-mode ABBs since it can process signals in the current domain and output signals in both voltage and current. VCII includes low-impedance input ports for current, high-impedance output ports for current, and low-impedance output ports for voltage. Voltage output first-order filtering topologies utilizing VCII have recently been published [19], [29], [30], [31]. The first-order filters proposed in [19], [29], and [30] provide only the low-pass response. The VCII-based first-order filter in [31] uses a dual-output VCII, three resistors, and a capacitor to generate a first-order all-pass filter. However, the VCII-based first-order filter in [31] uses two VCII with dual output current terminals (dual X terminals), which is not easy to implement by using a commercially available IC. Moreover, it provides only an all-pass response.

The purpose of this paper is to design a first-order multifunction filter using a VCII. This contribution is organized as follows: the operating concept is outlined in Section II, which also provides a brief review of VCII, 0.4 V VCII CMOS structure, the proposed reconfigurable multifunction filter, and an analysis of voltage/current gain errors and parasitic effects. The simulation results based on the CMOS VCII from Cadence program are shown in Section III. The simulation and experimental results based on the AD844-VCII are depicted in Section IV. Section V describes the modification to obtain electronic controllability. Finally, a brief conclusion is presented in Section VI.

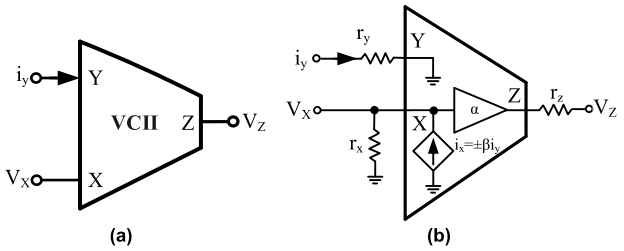


FIGURE 1. VCII, (a) symbolic representation (b) equivalent circuit.

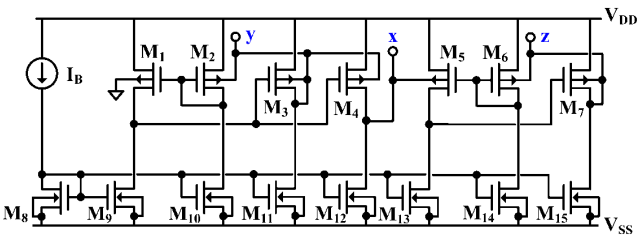


FIGURE 2. CMOS structure of the VCII.

II. PRINCIPLE OF OPERATION

A. OVERVIEW OF VCII

A versatile active building block, VCII is used to design the first-order multifunction filter. So, a brief review of this active building block is described in this section. The symbolic representation and equivalent circuit of a VCII are illustrated in Fig. 1(a) and (b), respectively. VCII's terminal voltage and current relationships are characterized by the following equation [8], [9], [10]:

$$\begin{pmatrix} i_x \\ v_y \\ v_z \end{pmatrix} = \begin{pmatrix} 1/r_x & \pm\beta & 0 \\ 0 & r_y & 0 \\ \alpha & 0 & r_z \end{pmatrix} \begin{pmatrix} v_x \\ i_y \\ i_z \end{pmatrix} \tag{1}$$

where β represents the current gain between Y and X terminals, and α represents the voltage gain between X and Z terminals. For the ideal case, both β and α are unity. The $-\beta$ denotes a VCII $-$ and $+\beta$ denotes a VCII+. According to (1), the Y terminal of VCII, unlike CCII, is a current input terminal with an ideal zero input impedance (ideally $r_y = 0$); the X terminal is a current output terminal with an ideal infinite impedance (ideally $r_x \rightarrow \infty$); and the Z terminal is a voltage output terminal with an ideal zero impedance (ideally $r_z = 0$). VCII can do current summing due to the availability of the current buffer at terminal Y, and it can also drive multiple loads according to the voltage buffer at port Z. The X terminal of VCII is also the voltage input terminal of the voltage buffer for copying to the voltage output terminal, Z [8], [9], [10].

B. 0.4 V VCII CMOS STRUCTURE

Figure 2 shows the CMOS structure of the low-voltage, low-power VCII [32]. The VCII structure is the combination of two unity-gain voltage/current buffers, firstly presented in [33] and confirmed experimentally in [34]. The Y-X current buffer is composed of transistors M_1-M_4 and M_9-M_{12} and ensures the unity gain current transfer $i_x = i_y$, while the voltage buffer X-Z is composed of transistors M_5-M_7 and M_{13}-M_{15} that ensures the unity gain voltage transfer $v_z = v_x$. Both buffers are based on a two-stage op-amp, operating in a closed-loop configuration. This op-amp is composed of the input non-tailed differential stage M_1-M_2 (M_5-M_6), followed by a second common-source stage with transistor M_3 (M_7). Note that the bulk terminal of the output transistor is shorted with its drain, which lowers the open-loop gain, but improves the overall accuracy of the voltage gain of the resulting voltage follower [33]. This is because such a connection provides $V_{TH2} = V_{TH3}$ ($V_{TH6} = V_{TH7}$) that entails concurrent voltage changes at the drains of the input transistors M_1 and M_2 (M_5 and M_6) for variations of the input voltage at the bulk terminal of M_1 (M_5).

$$V_{vXZ} = \frac{A_o}{1 + A_o} \tag{2}$$

where:

$$A_o \cong \frac{g_{mb5}}{g_{o5} + g_{o13}} \cdot \frac{g_{m7}}{g_{o7} + g_{o15}} \cdot \frac{1}{1 + g_{mb7}/g_{m7}} \tag{3}$$

thus, despite the loading of the output transistor M_3 (M_7) with its g_{mb}, the gain remains similar as for a two-stage unloaded OTA, operating in a voltage follower configuration. Consequently, the resulting gain error, with respect to unity, can be as low as 0.1-0.3 %. Nevertheless, the open loop gain remains relatively low, which simplifies frequency compensation and allows for avoiding a compensation capacitor for typical cases [33].

In the current follower buffer, the transistor M_4, identical with M_3, is added, thus repeating the current flowing through M_3, and providing a high-impedance output. Note that both V_{GS} and V_{BS} voltages for M_3 and M_4 must be equal to achieve equal drain currents. Also note that the whole current buffer M_1-M_4 and M_9-M_{12} can be seen as a second-generation current conveyor [34], with its voltage terminal, at the bulk terminal of M1, grounded. Thus, the proposed VCII can be seen as a connection of a current buffer based on a current conveyor and an additional precision voltage follower.

The bias current I_B and the transistor M_8 set the biasing current of the circuit. The circuit operates in weak inversion and employs the bulk-driven technique with a very simple topology, enabling rail-to-rail operation under an extremely low voltage supply, even much less than the threshold voltage of a single transistor ($V_{DDmin} = \max(V_{SG-M2} + V_{DSAT-M10})$ where V_{SG} and V_{DSsat} represent the source-gate voltage and saturation voltage of the MOS transistor, respectively). It is worth mentioning that the CMOS structure of the VCII has been used in a 0.5 V current-mode low-pass filter [32].

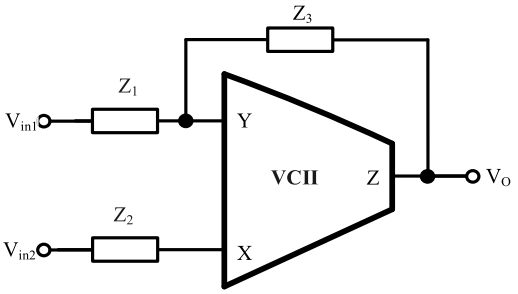


FIGURE 3. VCII-based voltage-mode first-order multifunction filter.

The output resistances of the y, x and z terminals are:

$$r_y \cong \frac{g_{o1} + g_{o9}}{g_{m3} g_{mb1}} \tag{4}$$

$$r_x \cong \frac{1}{g_{o4} + g_{o12}} \tag{5}$$

$$r_z \cong \frac{g_{o5} + g_{o13}}{g_{m7} g_{mb5}} \tag{6}$$

where g_m, g_{mb}, g_o are the transconductance, bulk transconductance and output conductance of the MOS transistor, respectively. The input referred thermal noise is determined by the input noise of the differential input stage:

$$\bar{v}_n^2 = 2\frac{2nkT}{g_{mb1}^2}\left(g_{m1,2} + g_{m9,10}\right) \tag{7}$$

where n is the subthreshold slope factor, k is the Boltzmann constant, and T is the temperature.

C. PROPOSED RECONFIGURABLE VOLTAGE-MODE FIRST-ORDER MULTIFUNCTION FILTER

The core structure of the proposed filter is depicted in Figure 3. It consists of one VCII and three passive elements, Z_1, Z_2, and Z_3. V_{in1} and V_{in2} are the input voltage nodes, and V_o is the voltage output node. The impedance Z_1 is connected between the input voltage node V_{in1} and the low impedance input current terminal Y. The impedance Z_2 is connected between the input voltage node V_{in2} and the high impedance output current terminal X and the impedance Z_3 is feedback from the voltage output terminal Z to the current input terminal Y. The voltage output node (V_o) of the proposed reconfigurable first-order filter is located at terminal Z, which ideally produces zero output impedance (r_z). As a result, without the employment of extra buffer devices, the filter designed in Fig. 3 can be cascaded to external loads as well as connected to the input node of next-stage circuits.

A simple analysis of the reconfigurable first-order voltage-mode versatile filter depicted in Figure 3 yields the following V_o equation:

$$V_O = \frac{Z_1 Z_3 V_{in2} - Z_2 Z_3 V_{in1}}{Z_1 (Z_2 + Z_3)} \tag{8}$$

Based on (8), the proposed circuit in Fig. 3 can be configured to achieve the first-order multifunction filter with three separate voltage-mode filtering responses (high-pass, low-pass, and all-pass) in the same topology.

TABLE 1. The filtering parameters of the proposed circuit type 1.

Input		Transfer function	Filtering Response	Gain	Phase	Pole Frequency
V_{in1}	V_{in2}					
1	0	$\frac{-\frac{R_f}{R_1}}{sCR_f+1}$	Inverting LPF	$\frac{R_f}{R_1}$	$180-\tan^{-1}\omega R_f C$	$\frac{1}{CR_f}$
0	1	$\frac{sCR_f}{sCR_f+1}$	Non-inverting HPF	1	$90-\tan^{-1}\omega R_f C$	
1	1	$\frac{sCR-1}{sCR+1}$ where $R_f=R_1=R$	Inverting APF (Leading Phase)	1	$180-2\tan^{-1}\omega RC$	

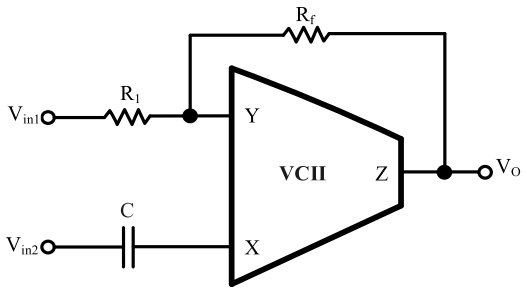


FIGURE 4. VCII-based MISO voltage-mode filter circuit type 1.

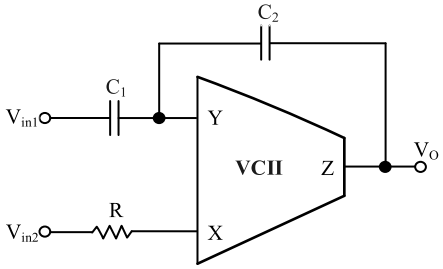


FIGURE 5. VCII-based MISO voltage-mode filter circuit type 2.

The input impedances at input voltage nodes, V_{in1} and V_{in2} and output impedance are ideally as follows:

$$Z_{in1}\,|_{V_{in2}=0} = Z_1 \tag{9}$$

$$Z_{in2}\,|_{V_{in1}=0} = Z_2 + Z_3 \tag{10}$$

and

$$Z_o\,|_{V_{in1}=V_{in2}=0} = 0 \tag{11}$$

The details for configuration are as follows:

1) THE PROPOSED FIRST-ORDER MULTIFUNCTIONAL FILTER: TYPE 1

The first type of the first-order voltage-mode multifunction filter is obtained by replacing the passive elements Z_1, Z_2, and Z_3 in the circuit scheme depicted in Fig. 3 by the resistor R_1, capacitor C, and resistor R_f, respectively. With

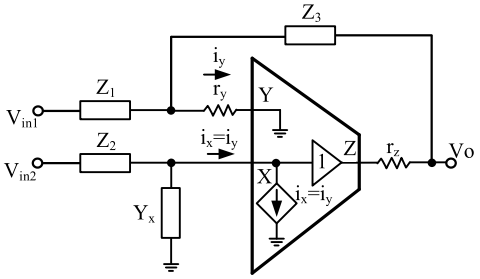


FIGURE 6. Proposed VCII-based first-order multifunction filter with parasitic elements.

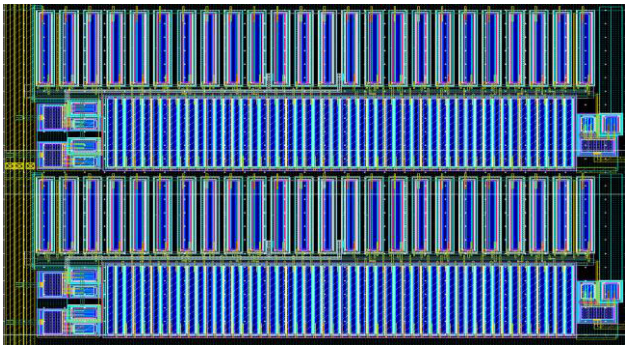


FIGURE 7. The layout of the VCII.

this configuration, it yields the first type of the first-order voltage-mode multifunction filter as depicted in Fig. 4. The following V_o equation results from a routine analysis of the VCII-based voltage-mode first-order versatile filter depicted in Figure 4:

$$V_o = \frac{sCR_f V_{in2} - \frac{R_f}{R_1} V_{in1}}{sCR_f + 1} \tag{12}$$

As illustrated in (12), the input voltage signal can be applied to the proper nodes, V_{in1} and V_{in2}, in order to offer three typical first-order filtering functions: LPF, HPF, and APF responses. Table 1 displays the filter response selections for proposed circuit type 1, where 1 indicates applying the input

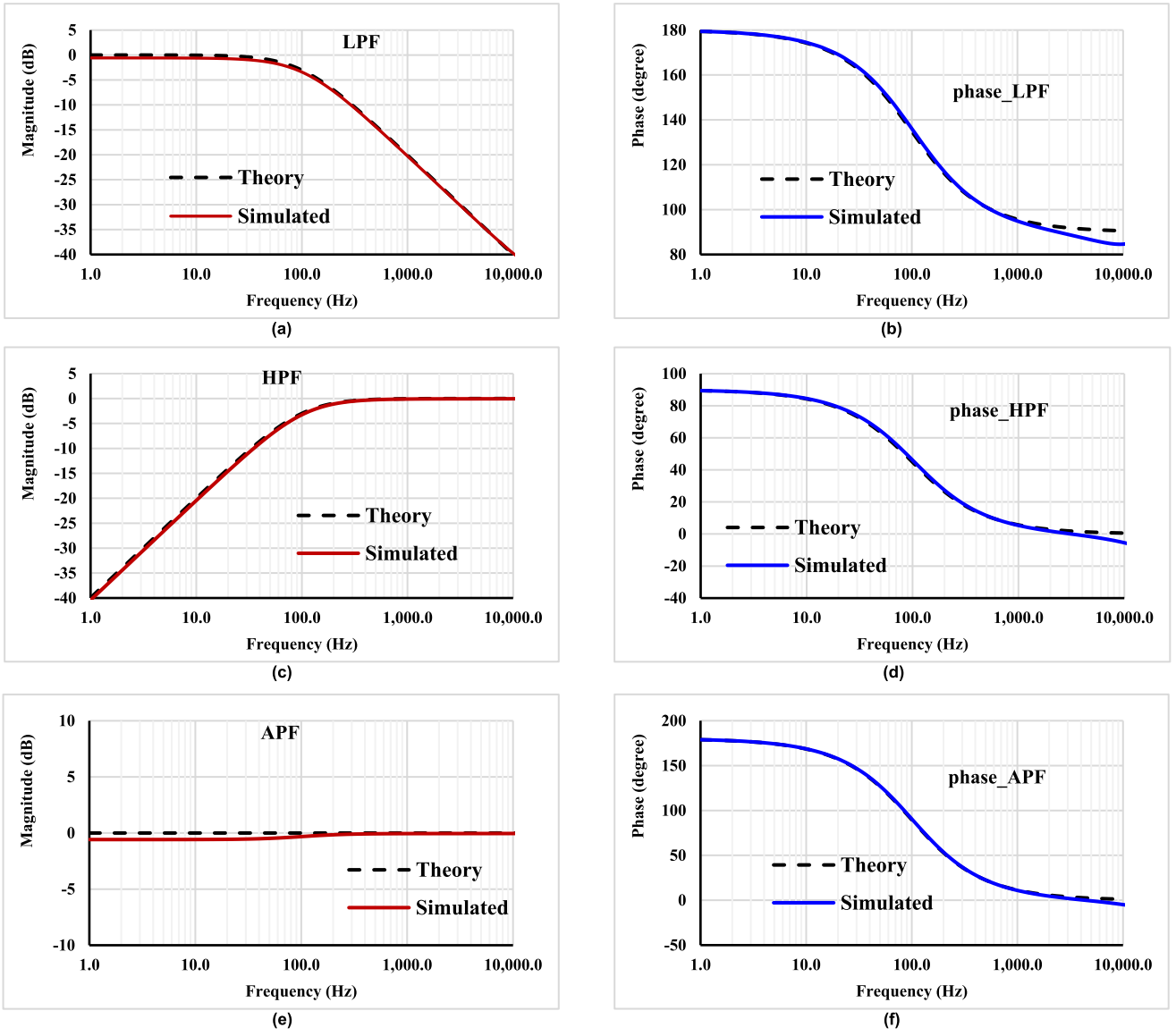


FIGURE 8. Frequency gain (a), (c), (e) and phase (b), (d), (f) responses of LPF, HPF, APF circuit type 1.

signal to that input voltage node, and 0 indicates connecting that input voltage node to the ground. The filtering parameters are also included in Table 1. It should be noted that the pass-band gain of the LPF function for circuit type 1 is controlled by R_1 without affecting the pole frequency. This controllable feature will be used in many applications. For example, in the first-order LPF-based multiphase sinusoidal oscillator, the condition of oscillation can be adjusted via the pass-band gain without affecting the frequency of oscillation. The APF for circuit type 1 provides the leading phase phenomenon.

2) THE PROPOSED FIRST-ORDER MULTIFUNCTIONAL FILTER: TYPE 2

The second type of the proposed first-order multifunction filter is obtained by replacing the passive elements Z_1, Z_2, and Z_3 in the circuit shown in Fig. 2 by the capacitor C_1, resistor R, and capacitor C_2, respectively. With this configuration, it yields the second type of the first-order voltage-mode multifunction filter as depicted in Fig. 5. A routine analysis of the VCII-based voltage-mode first-order multifunction filter depicted in Figure 5 yields the following output voltage equation:

$$V_o = \frac{V_{in2} - sC_1RV_{in1}}{sC_2R + 1} \tag{13}$$

As illustrated in (13), the input voltage signal can be applied to the proper nodes, V_{in1} and V_{in2}, in order to offer three typical first-order filtering functions: LPF, HPF, and APF responses. The filter response selections for the proposed circuit type 2 are shown in Table 2. The filtering parameters are also included in Table 2. It should be noted that the pass-band gain of the HPF function for circuit type 2 is controlled by C_1 without affecting the pole frequency. This controllable

TABLE 2. The filtering parameters of the proposed circuit type 2.

Input V_{in1}	Input V_{in2}	Transfer function	Filtering Response	Gain	Phase	Pole Frequency
0	1	$\frac{1}{sC_2R+1}$	Non-inverting LPF	1	$-\tan^{-1}\omega C_2R$	$\frac{1}{C_2R}$
1	0	$-\frac{sC_1R}{sC_2R+1}$	Inverting HPF	$\frac{C_1}{C_2}$	$-90-\tan^{-1}\omega C_2R$	
1	1	$\frac{-sCR+1}{sCR+1}$ where $C_1=C_2=C$	Non-inverting APF (Lagging Phase)	1	$-2\tan^{-1}\omega CR$	

TABLE 3. The filtering parameters with the effect of the current and voltage gain errors for circuit type 1.

Input V_{in1}	Input V_{in2}	Transfer function	Filtering Response	Gain	Phase	Pole Frequency
1	0	$\frac{-\beta\frac{R_f}{R_1}}{s\frac{CR_f}{\alpha}+\beta}$	Inverting LPF	$\frac{R_f}{R_1}$	$180-\tan^{-1}\frac{\omega R_fC}{\alpha\beta}$	$\frac{\alpha\beta}{CR_f}$
0	1	$\frac{sCR_f}{s\frac{CR_f}{\alpha}+\beta}$	Non-inverting HPF	α	$90-\tan^{-1}\frac{\omega R_fC}{\alpha\beta}$	
1	1	$\frac{sCR-\beta}{s\frac{CR}{\alpha}+\beta}$ where $R_f=R_1=R$	Inverting APF (Leading Phase)	$\frac{\sqrt{(\omega CR)^2+\beta^2}}{\sqrt{\left(\frac{\omega CR}{\alpha}\right)^2+\beta^2}}$	$\left(180-\tan^{-1}\frac{\omega RC}{\beta}-\tan^{-1}\frac{\omega RC}{\alpha\beta}\right)$	

TABLE 4. The filtering parameters with the effect of the current and voltage gain errors for circuit type 2.

Input V_{in1}	Input V_{in2}	Transfer function	Filtering Response	Gain	Phase	Pole Frequency
0	1	$\frac{1}{\beta sC_2R+\frac{1}{\alpha}}$	Non-inverting LPF	α	$-\tan^{-1}\alpha\beta\omega C_2R$	$\frac{1}{\alpha\beta C_2R}$
1	0	$\frac{-\beta sC_1R}{\beta sC_2R+\frac{1}{\alpha}}$	Inverting HPF	$\frac{C_1}{C_2}$	$-90-\tan^{-1}\alpha\beta\omega C_2R$	
1	1	$\frac{-\beta sCR+1}{\beta sCR+\frac{1}{\alpha}}$ where $C_1=C_2=C$	Non-inverting APF (Lagging Phase)	$\frac{\sqrt{(\beta\omega CR)^2+1}}{\sqrt{(\beta\omega CR)^2+\left(\frac{1}{\alpha}\right)^2}}$	$-\left(\tan^{-1}\beta\omega CR+\tan^{-1}\alpha\beta\omega CR\right)$	

feature will be used in many applications. For example, in the first-order HPF-based multiphase sinusoidal oscillator, the condition of oscillation can be adjusted via the pass-band gain without affecting the frequency of oscillation. The APF for circuit type 2 provides the lagging phase phenomenon.

D. STUDY OF CURRENT/VOLTAGE GAIN ERRORS AND PARASITIC EFFECTS

First, the effect of current and voltage gain errors from the input terminals to the output terminals of VCII is studied. The β and α are defined as the current gain error between

TABLE 5. The filtering parameters involving parasitic effect for circuit type 1.

Input V_{in1}	Input V_{in2}	Transfer function	Filtering Response	Gain	Phase	Pole Frequency
1	0	$\frac{-\frac{R_f}{R_1}}{sCR^*+1}$	Inverting LPF	$\frac{R_f}{R_1}$	$180-\tan^{-1}R^*C$	$\frac{1}{CR^*}$
0	1	$\frac{sCR^*}{sCR^*+1}$	Non-inverting HPF	1	$\tan^{-1}\frac{1}{R^*C}$	
1	1	$\frac{sCR^*-\frac{R_f}{R_1}}{sCR^*+1}$	Inverting APF (Leading Phase)	$\frac{\sqrt{\left(\omega CR^*\right)^2+\left(\frac{R_f}{R_1}\right)^2}}{\sqrt{\left(\omega CR^*\right)^2+1}}$	$\begin{pmatrix}180-\tan^{-1}\frac{\omega R_1R^*C}{R_f}-\\ \tan^{-1}\omega R^*C\end{pmatrix}$	

* Not that $R^*=R_f+r_y\left(1+\frac{R_f}{R_1}\right)$.

TABLE 6. The filtering parameters involving parasitic effect for circuit type 2.

Input V_{in1}	Input V_{in2}	Transfer function	Filtering Response	Gain	Phase	Pole Frequency
0	1	$\frac{sA+1}{sB+1}$	Non-inverting LPF	1 (Considering at low frequency)	$\tan^{-1}(A)-\tan^{-1}(B)$	$\frac{1}{B}$
1	0	$\frac{-sC_1R}{sB+1}$	Inverting HPF	$\frac{C_1R}{B}$	$-90-\tan^{-1}(B)$	
1	1	$\frac{sA+1-sC_1R}{sB+1}$	Non-inverting APF (Lagging Phase)	$\frac{\sqrt{\left(\omega A-\omega C_1R\right)^2+1}}{\sqrt{\left(\omega B\right)^2+1}}$	$-\begin{bmatrix}\tan^{-1}(\omega C_1R-A)+\\ \tan^{-1}B\end{bmatrix}$	

* Note that $A=C_1r_y\left(1+\frac{C_2}{C_1}\right)$ and $B=C_2R+C_1r_y\left(1+\frac{C_2}{C_1}\right)$. The parasitic resistance r_y causes the extra zero with the following zero frequency $f_z=\frac{1}{2\pi C_1r_y\left(1+\frac{C_2}{C_1}\right)}$. The extra zero mostly affect the performance of the LPF filter.

Y and X terminals and the voltage gain error between X and Z terminals, respectively. A straightforward analysis of the first-order multifunction circuit designed in Figure 3 with these current and voltage gain errors provides the following output voltage equation:

$$V_O=\frac{Z_1Z_3V_{in2}-\beta Z_2Z_3V_{in1}}{Z_1\left(\beta Z_2+\frac{Z_3}{\alpha}\right)} \tag{14}$$

The output voltage equation for the proposed first voltage-mode multifunction filter (Fig. 4) with the effect of current and voltage gain errors is given by:

$$V_o=\frac{sCR_fV_{in2}-\beta\frac{R_f}{R_1}V_{in1}}{s\frac{CR_f}{\alpha}+\beta} \tag{15}$$

From (14), the filtering parameters with the effects of the current and voltage gain errors are summarized in Table 3.

For the proposed second voltage-mode multifunction filter (Fig. 5), the output voltage equation with the effect of the current and voltage gain errors is given by

$$V_o=\frac{V_{in2}-\beta sC_1RV_{in1}}{\beta sC_2R+\frac{1}{\alpha}} \tag{16}$$

From (16), the filtering parameters with the effect of the current and voltage gain errors are summarized in Table 4.

The effect of parasitic elements on filtering performance will be investigated later. Figure 6 depicts a model of the proposed filter with parasitic elements in VCII. If the load resistance connected at the output voltage node *Vo* is much larger than the resistance at the terminal Z ($R_L \gg r_z$), and ignoring r_z, the following output voltage is obtained:

$$V_o=\frac{\left[r_y\left(Z_1+Z_3\right)+Z_1Z_3\right]V_{in2}-Z_2Z_3V_{in1}}{Z_1Z_2+\left[r_y\left(Z_1+Z_3\right)+Z_1Z_3\right]\left(1+Y_XZ_2\right)} \tag{17}$$

where $Y_X=sC_X//G_X$.

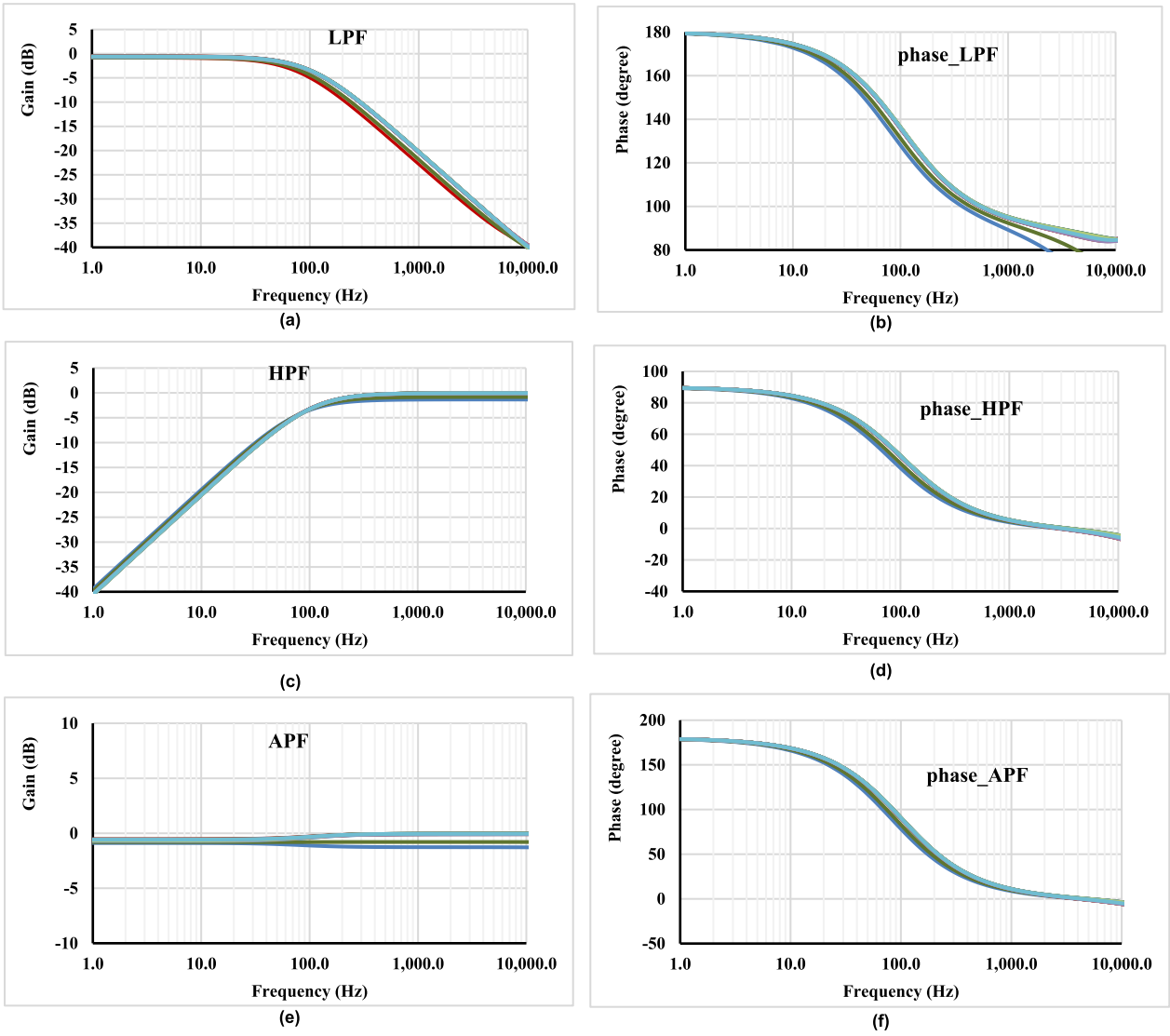


FIGURE 9. Frequency gain (a), (c), (e) and phase (b), (d), (f) responses of LPF, HPF, APF circuit type 1 with PVT corners analysis.

It is found from (17) that the parasitic capacitance and resistance (Y_x) at terminal X cause the extra pole. This extra pole frequency limits the operation of the proposed circuit at high frequency and is given by $f_p = 1/[2\pi C_x(Z_2 \,//r_x)]$. The output voltage equation for the proposed first multifunction filter (Fig. 4) with the parasitic effects is given by

$$V_o = \frac{sC\left[R_f + r_y\left(1+\frac{R_f}{R_1}\right)\right]V_{in2} - \frac{R_f}{R_1}V_{in1}}{sC\left[R_f + r_y\left(1+\frac{R_f}{R_1}\right)\right]+1} \tag{18}$$

where Y_x is ignored. The filtering parameters involving parasitic impacts from (18) are summarized in Table 5.

From (17), the output voltage equation for the proposed second voltage-mode multifunction filter (Fig. 5) with the parasitic effects is given by

$$V_o = \frac{\left[sC_1r_y\left(1+\frac{C_2}{C_1}\right)+1\right]V_{in2} - sC_1RV_{in1}}{s\left[C_2R + C_1r_y\left(1+\frac{C_2}{C_1}\right)\right]+1} \tag{19}$$

where Y_x is ignored. The filtering parameters involving parasitic impacts from (19) are summarized in Table 6.

III. POST-LAYOUT SIMULATION RESULTS BASED ON THE CMOS VCII

The VCII is designed in Cadence program using the 0.18μm CMOS technology from TSMC. The voltage supply is 0.4V ($\pm$0.2V), the bias current is 25nA, and the power consumption of the VCII is 383 nW. The transistors aspect ratio in μm/μm are for M_1, M_2, M_5, M_6, M_8 =50/1, M_3, M_4, M_7 =5 $\times$ 50.1, M_9, M_{10}, M_{13}, M_{14} =100/1, M_{11}, M_{12}, M_{15} =5 $\times$ 100.1. The chip area of the VCII is 0.0221mm^2. The layout of VCII is depicted in Fig. 7.

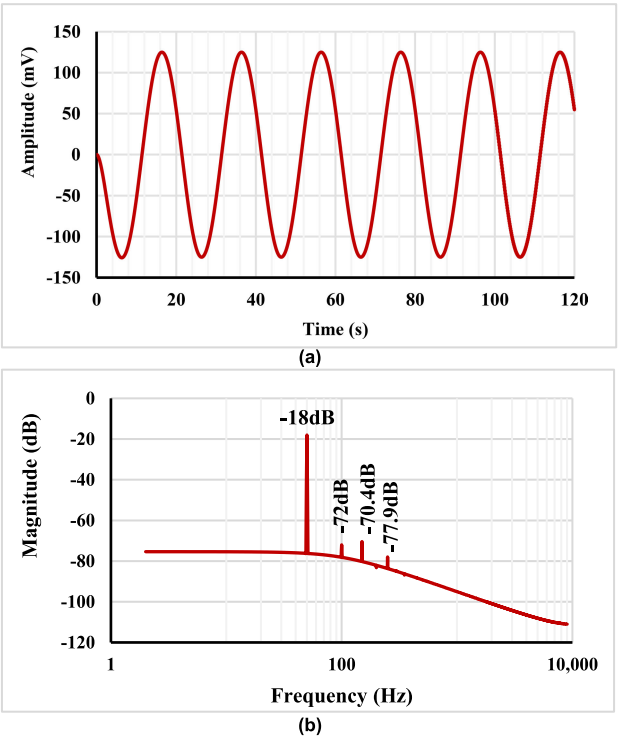


FIGURE 10. The transient analysis of the LPF output (a) and its FFT (b).

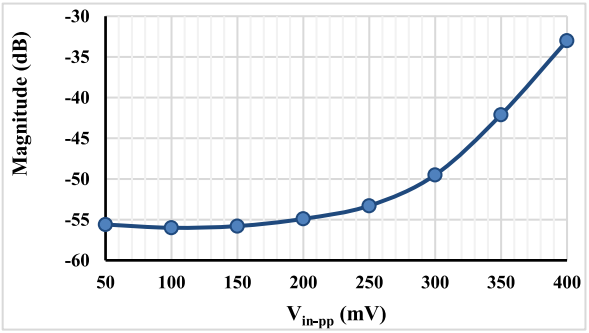


FIGURE 11. The THD for the LPF output signal for different V_{in-pp}.

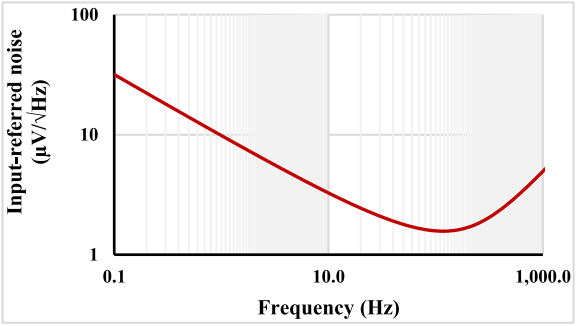


FIGURE 12. The input referred noise of the LPF.

A. THE PROPOSED FIRST-ORDER FILTER: TYPE 1

For the first filter, the values of the passive components were $R_1 = R_f = 800$ kΩ, $C = 2$nF and the load capacitance $C_L = 2$pF. The frequency gain and the phase responses for the LPF, HPF and APF are shown in Figs. 8 (a) to (f). The calculated pole frequency f_0 was 99.52 Hz, and it is very close to the simulated one 100 Hz.

To confirm the robustness of the designed VCII-based filter under process, voltage, and temperature (PVT) corners, the simulation results of the fast-fast, fast-slow, slow-fast, and slow-slow process corners, the voltage supply with ±10% variation and temperature corners -40°C and 70°C are shown in Fig. 9 (a) to (f). It can be concluded that the deviations are acceptable for the proper circuit operation. The transient analysis of the output signal and its fast Fourier transfer (FFT) of the LPF with applied input voltage V_{inpp} =300mV @ 50Hz is shown in Fig. 10. The total harmonic distortion (THD) is -49.5 dB. Fig. 11 shows the THD of the output signal for different applied input signals @ 50Hz. It is evident that the filter can process input signals near to rail-to-rail with low THD. The input-referred noise of the LPF is shown in Fig. 12. The input-referred noise is 24 μV_{rms}, which results in a dynamic range (DR) of 72.9 dB for 1% THD.

B. THE PROPOSED FIRST-ORDER FILTER: TYPE 2

For the second filter, the values of the passive components were $R = 800$ kΩ, $C_1 = C_2 = 2$nF and $C_L = 2$pF. The frequency gain and the phase responses for the LPF, HPF and APF are shown in Fig. 13 (a) to (f), respectively. The calculated pole frequency f_0 was 99.52 Hz, and it is very close to the simulated one 100 Hz. It is seen that the simulated responses for LPF deviate from the theoretical responses at frequencies higher than 2kHz. This critical deviation is caused by the parasitic and non-ideal gain effects of the VCII.

IV. SIMULATION AND EXPERIMENTAL RESULTS BASED ON THE AD844-VCII

A. THE PROPOSED FIRST-ORDER FILTER: TYPE 1

In this section, simulation and experimental investigations are carried out to validate the performance of Figure 4's proposed first-order multifunctional filter. The simulated and experimental tests utilize AD844 constructed as VCII. The proposed first-order filter type 1 is simulated and experimentally tested in both the time and frequency domains with ±5 V power supplies. The capacitor, $C = 1$nF, and the resistors, $R_1 = R_f = 2$kΩ are the components used in the proposed first-order filter type 1. The ideal pole frequency calculated from these components is 79.5kHz. As shown in Table 1, the input signal is applied to the input voltage nodes, V_{in1}, V_{in2}, to provide three standard first-order filtering functions: low-pass, high-pass, and all-pass responses. For the first test, the input voltage signal is applied at node V_{in1} to obtain the LPF function. Figure 14 shows the LPF frequency gain and phase responses obtained from the simulation and experiment. The simulated and experimental natural frequencies are 78.9 kHz (0.7% error) and 79.3 kHz (0.2% error), respectively. It is clearly seen that the experimental responses deviate from the simulated and theoretical responses at frequencies higher than 1 MHz. This deviation causes the current/voltage gain errors and parasitic

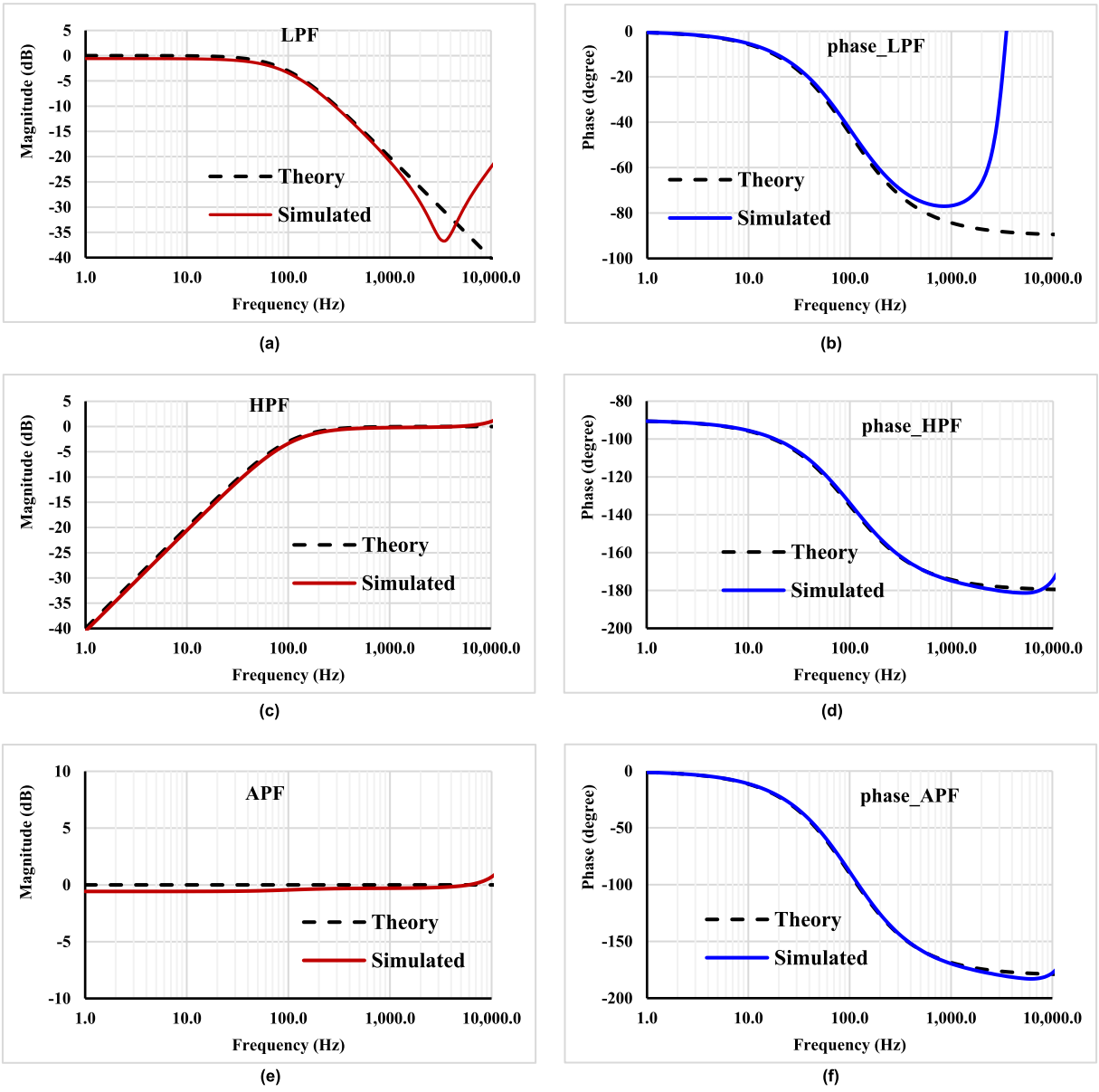


FIGURE 13. Frequency gain (a), (c), (e) and phase (b), (d), (f) responses of LPF, HPF, APF circuit type 2.

resistance/capacitances in VCII, as predicted in Section II-D, as well as the tolerance of passive components, wire connections, breadboards, etc. Secondly, the input voltage signal is applied at node V_{in2} to obtain the HPF function.

Figure 15 shows the HPF frequency gain and phase responses obtained from the simulation and experiment. The simulated and experimental natural frequencies are 79.4kHz (0.1% error) and 79.8kHz (0.3% error), respectively. Thirdly, the input voltage signal is applied at nodes V_{in1} and V_{in2} to obtain the leading phase APF function. Figure 16 shows the leading phase APF frequency gain and phase responses obtained from the simulation and experiment. The simulated and experimental natural frequencies are 79.2kHz (0.3% error) and 79.4kHz (0.1% error), respectively. Time domain analyses of LPF, HPF and APF for the first-order multifunctional filter type 1 are respectively shown in Figs. 17, 18, and 19, where a sinusoidal input voltage with peak-to-peak 100mV at the frequencies 10kHz, 80kHz and 100kHz.

B. THE PROPOSED FIRST-ORDER FILTER: TYPE 2

The proposed filter (type 2) depicted in Fig. 5, is simulated, and experimentally tested in both the time and frequency domains with ±5 V power supplies. $C_1 = C_2 = 1$nF, $R = 2$ kΩ are the components used in circuit type 1. The ideal pole frequency calculated from these components is 79.5kHz. As shown in Table 2, the input signal is applied to the input voltage nodes, V_{in1}, V_{in2}, to provide three standard first-order filtering functions: low-pass, high-pass, and all-pass responses. The input voltage signal is applied at node

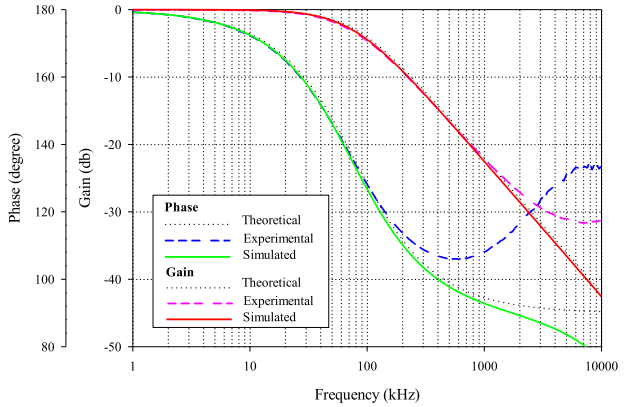


FIGURE 14. Simulated and experimental gain and phase response of LPF circuit type 1.

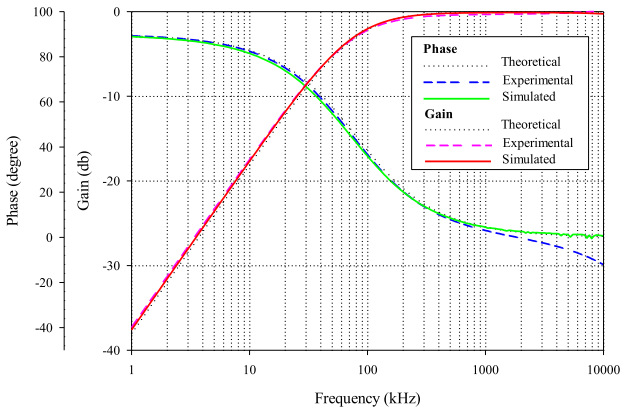


FIGURE 15. Simulated and experimental gain and phase response of high-pass circuit type 1.

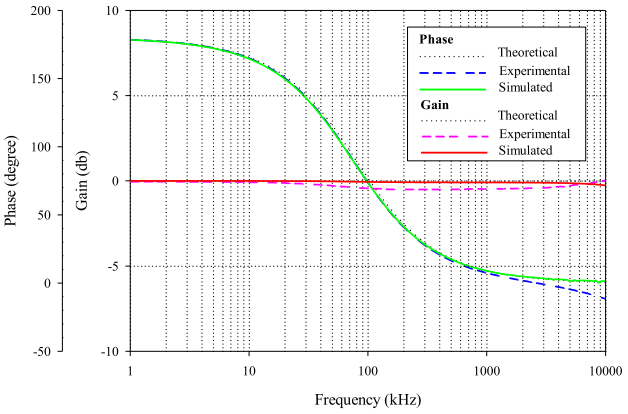
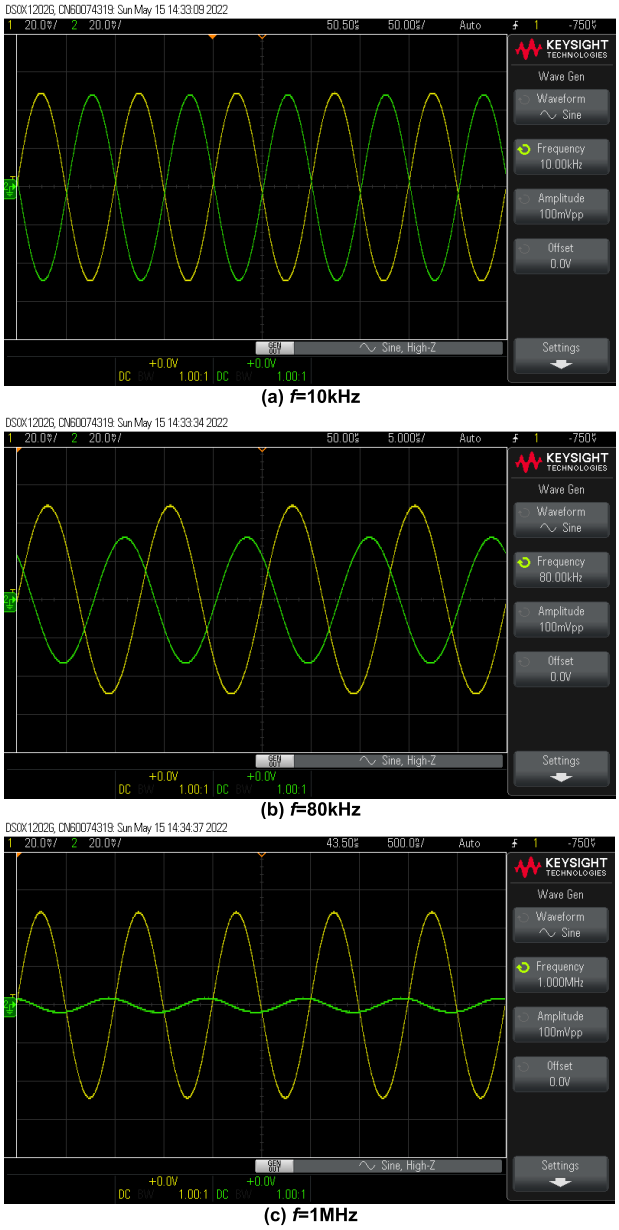


FIGURE 16. Simulated and experimental gain and phase response of all-pass circuit type 1.

V_{in2} to obtain the non-inverting LPF function. Figure 20 shows the LPF frequency gain and phase responses obtained from the simulation and experiment. The simulated and experimental natural frequencies are 79.6kHz (0.1% error) and 79.5kHz (0% error), respectively. It is clearly seen that the simulated and experimental responses deviate from the theoretical responses at frequencies higher than 1 MHz.

When the input voltage signal is applied at the input voltage node V_{in2}, the HPF function is obtained. Figure 21 shows the



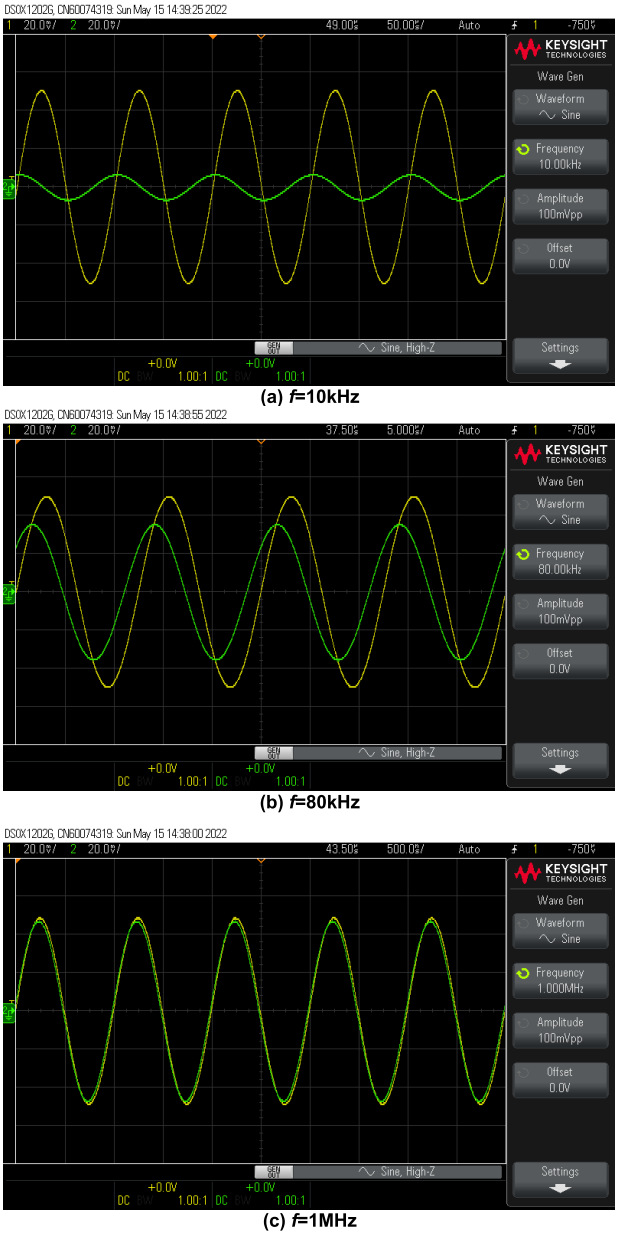
(a) f=10kHz

(b) f=80kHz

(c) f=1MHz

FIGURE 17. Time domain experimental result of inverting V_{LP} and V_{in} (—V_{in}, – – – V_{LP}) where$R_1 = R_f = 2k\Omega$, C = 1nF.

inverting HPF frequency gain and phase responses obtained from the simulation and experiment. In this result, the simulated and experimental natural frequencies are 79.8kHz (0.3% error) and 79.3kHz (0.2% error), respectively. When the input voltage signal is applied at the input voltage nodes V_{in1} and V_{in2}, the lagging phase APF function is obtained. Figure 22 shows the lagging phase APF frequency gain and phase responses obtained from the simulation and experiment. The simulated and experimental natural frequencies are 79.4kHz (0.1% error) and 79.1kHz (0.5% error), respectively. Time domain analyses of LPF, HPF and APF for the proposed first-order filter type 2 are respectively shown in Figs. 23, 24, and 25, where a sinusoidal input

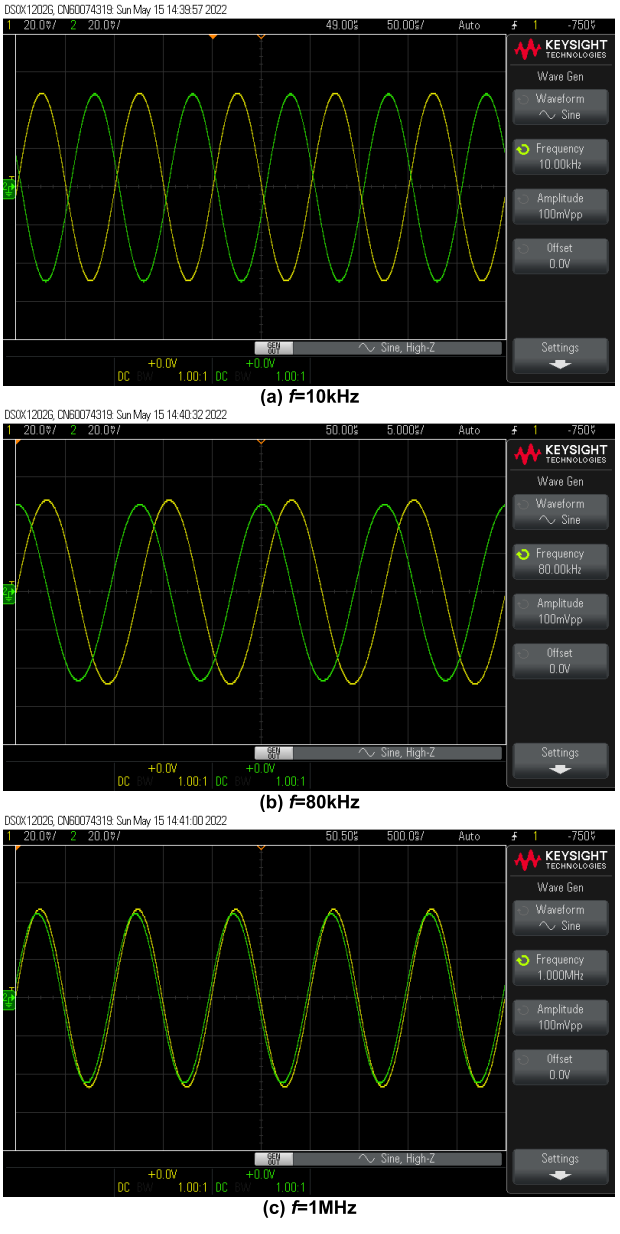


(a) f=10kHz

(b) f=80kHz

(c) f=1MHz

FIGURE 18. Time domain experimental result of non-inverting V_{HP} and V_{in} (– – – –V_{in}, – – – – V_{HP}) where$R_1 = R_f = 2k\Omega$, C = 1nF.



(a) f=10kHz

(b) f=80kHz

(c) f=1MHz

FIGURE 19. Time domain experimental result of inverting V_{AP} and V_{in} (– – – –V_{in}, – – – – V_{AP}) where$R_1 = R_f = 2k\Omega$, C = 1nF.

voltage with peak-to-peak 100mV at the frequencies 10kHz, 80kHz and 100kHz.

V. THE MODIFICATION FOR ACHIEVING ELECTRONIC CONTROLLABILITY

Recently, the designs of electronically controllable analog circuits have been receiving a lot of attention. The electronic controllability feature, which is easily controlled by a microcontroller or microcomputer, is required for modern circuits. So, the second type of the proposed first-order allpass filter is modified to achieve electronic controllability by replacing the passive resistor R with an OTA-based circuit as depicted in Fig. 26. If $C_1 = C_2 = C$, the following output voltage equation is obtained

$$\frac{V_o}{V_{in}} = \frac{-sC + g_m}{sC + g_m} \tag{20}$$

From (20), the lagging phase shift is electronically tuned via g_m.

The modified allpass filter with electronic controllability is tested by PSpice simulator tool and experiment verification utilizing the LT1228-based OTA and AD844-based VCII. Figure 27 displays the simulated and experimental results for various I_B values of 15 μA, 35 μA and 72 μA where $C_1 = C_2 = 1$nF and ± 5 supply voltages. The results revealed that the phase shift of APF is electronically controllable, as expected in (16). At $f = 79.5$ kHz, these I_B values

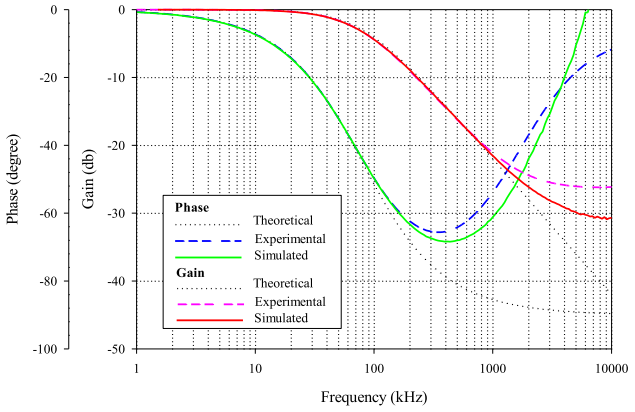


FIGURE 20. Simulated and experimental gain and phase response of LPF circuit type 2.

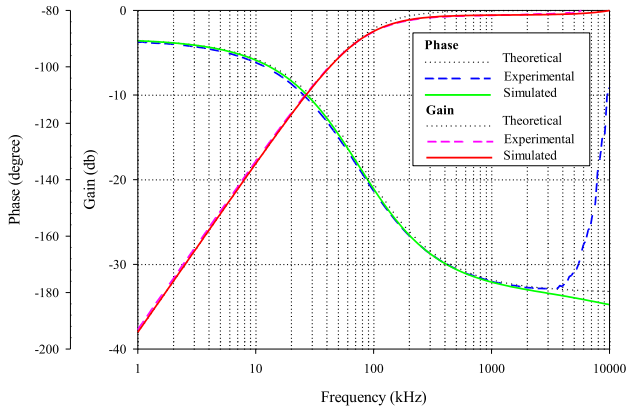


FIGURE 21. Simulated and experimental gain and phase response of high-pass circuit type 2.

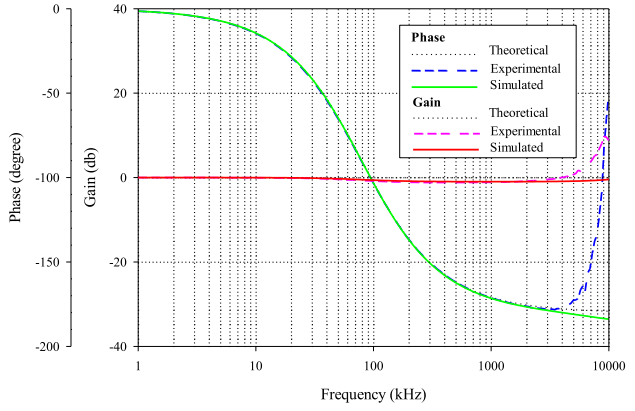
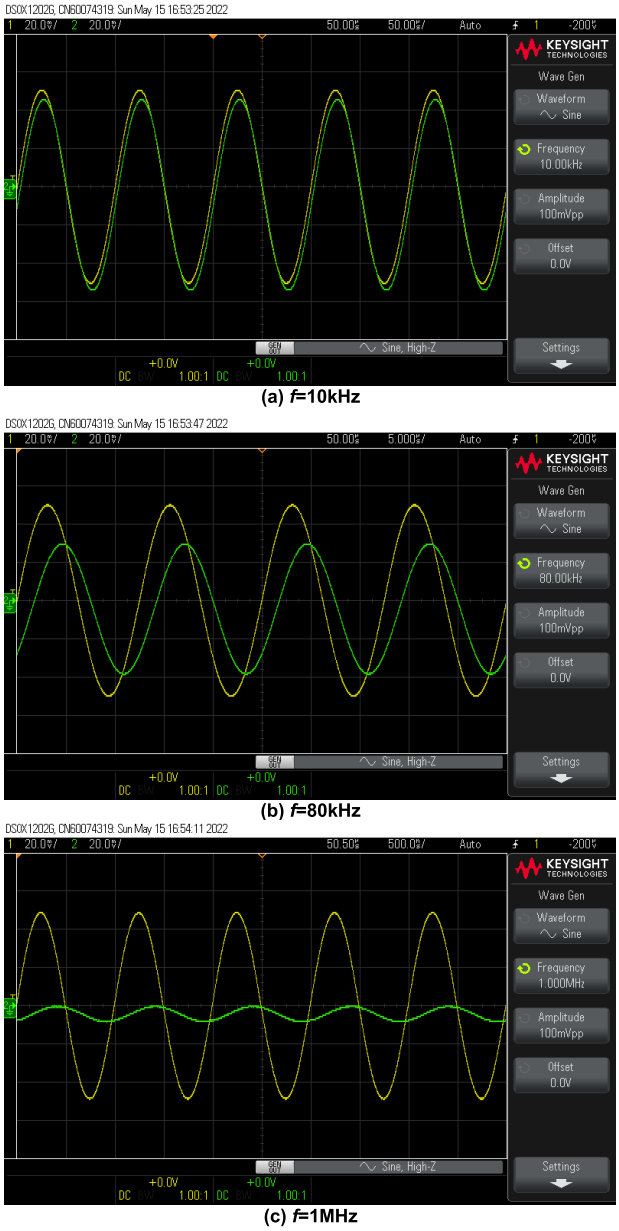


FIGURE 22. Simulated and experimental gain and phase response of all-pass circuit type 2.

result in simulated phase angles of −146.06°, −110.53°, and −70.47°, respectively, while the theoretical phase angles are −149.14°, −112.3°, and −71.49°, respectively. From these I_B values, the percent errors in the simulated phase angles are 2.11%, 1.77 %, and 1.45%. From these I_B values, the experimental phase angles at f= 79.5 kHz are −154.58°, −116.07°, and −73.81°, respectively. The experimental phase angles deviated from these I_B values by 3.65%, 3.36%,



(a) f=10kHz

(b) f=80kHz

(c) f=1MHz

FIGURE 23. Time domain experimental result of non-inverting V_{LP} and V_{in} (V_{in}, V_{LP}) of circuit type 2 where $C_1 = C_2 = 1$nF R = 2kΩ.

and 3.25%, respectively. Figure 28 illustrates the measured input and output waveforms of an all-pass filter with varied I_B values of 15 μA, 35 μA and 72 μA when the amplitude of the input signal is 50 mV_{pp} @ 10kHz.

Table 7 compares the proposed filters to those previously published [19], [29], [30], [31] with a first filter. The proposed filter has a lower supply voltage and lower power consumption than [29], [30], [31]. The VCII-based first-order filter presented in references [19] and [31] employs two VCII with dual output current terminals (dual DO-VCII), which is difficult to achieve using a commercially available integrated circuit. In [19] and [31], four passive elements are required for the first-order filter. The first-order filters presented

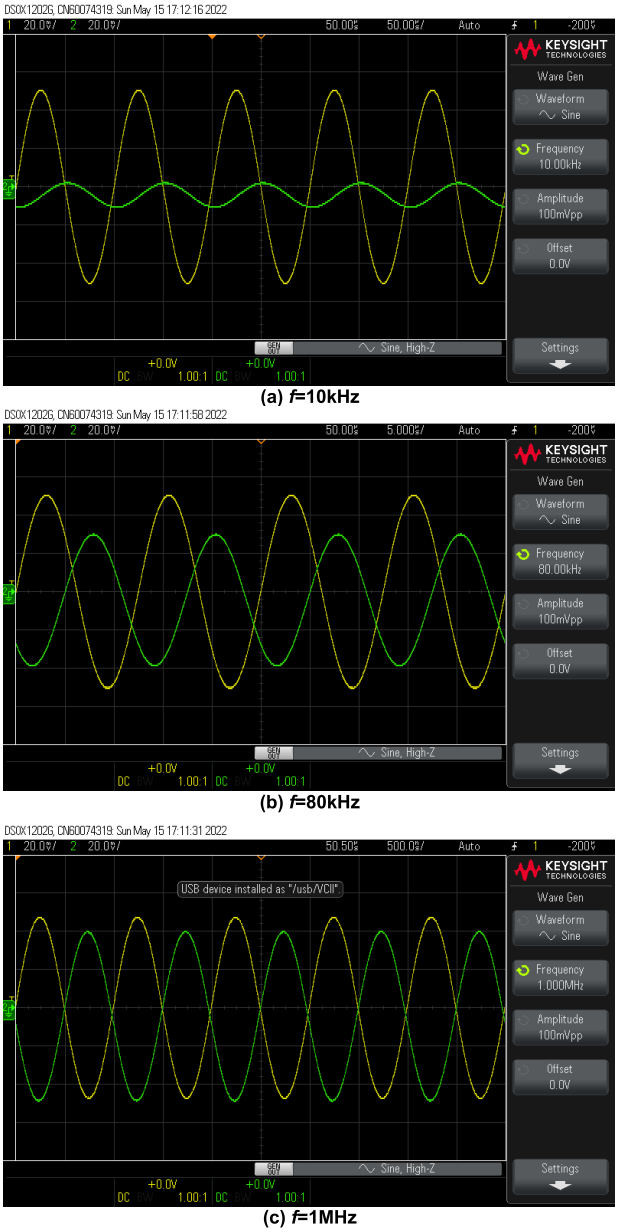


FIGURE 24. Time domain experimental result of inverting V_{HP} and V_{in} (– – – –V_{in}, – – – – V_{HP}) of circuit type 2 where $C_1 = C_2 = 1nF$ $R = 2k\Omega$.

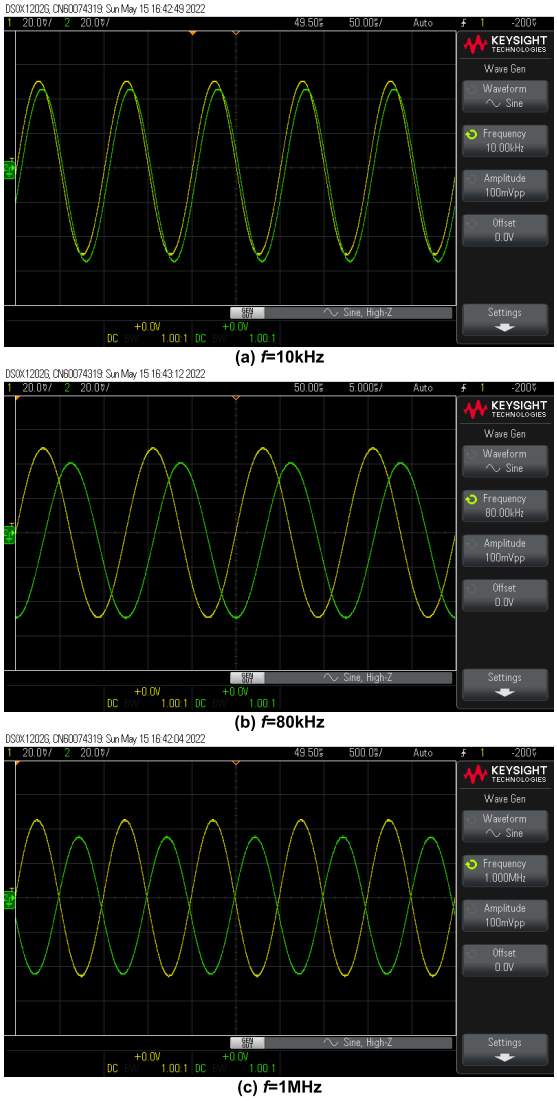


FIGURE 25. Time domain experimental result of non-inverting V_{AP} and V_{in} (– – – –V_{in}, – – – – V_{AP}) of circuit type 2 where $C_1 = C_2 = 1nF$ $R = 2k\Omega$.

in [19], [29], and [30] offer just the LPF response, whereas [31] provides only the NAPF response. Additionally, the recent multifunctional first-order filters [35], [36], [37] based on different active elements are also compared in Table 7. The proposed filter still has the lowest voltage supply.

VI. APPLICATION EXAMPLE AS QUADRATURE SINEWAVE OSCILLATOR

The VCII-based MISO voltage-mode first-order filter (circuit type-2) depicted in Fig. 5 is used as a sub-circuit to synthesize the quadrature sinusoidal oscillator. By connecting the type 2 first-order filter and the inverting lossless integrator, the completed voltage-mode sinusoidal oscillator is shown in Fig. 29. The output voltage nodes, V_{O1} and

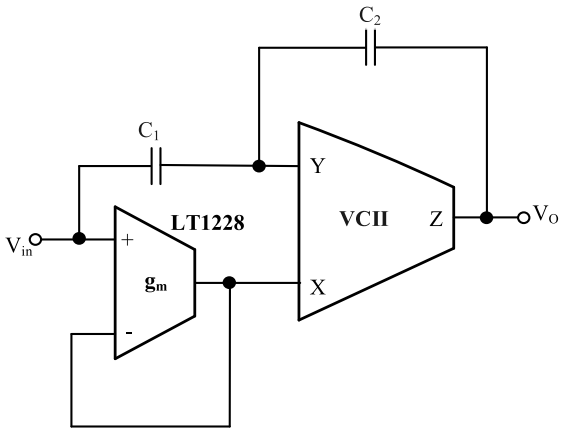


FIGURE 26. The modified allpass filter with electronic controllability.

V_{O2} for the quadrature sinusoidal output, are low impedance. The characteristic equation of the proposed oscillator is

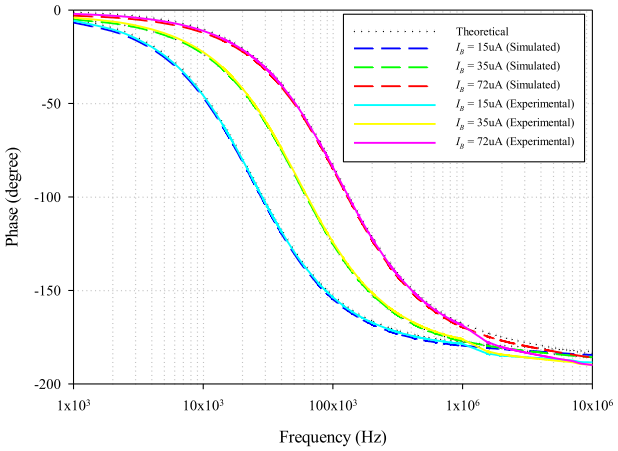
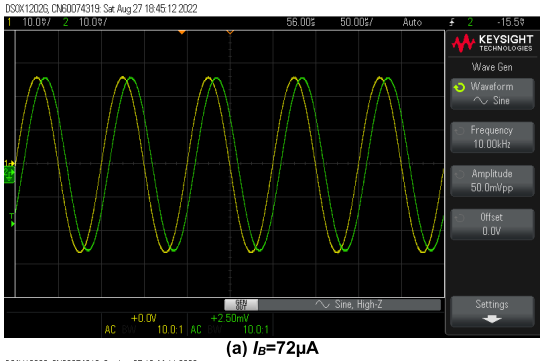
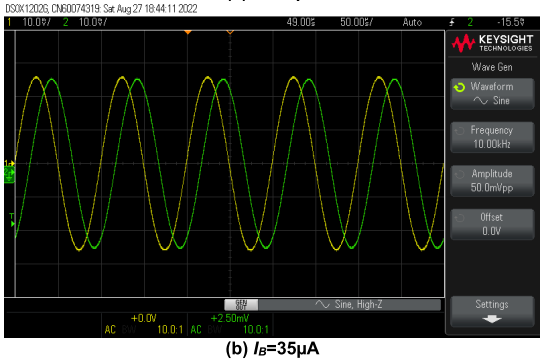


FIGURE 27. The modified allpass filter with electronic controllability.





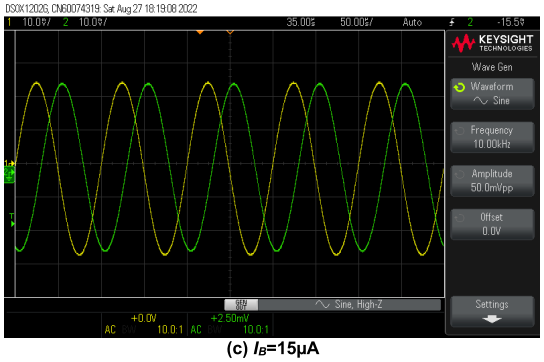


FIGURE 28. Input and output waveforms (– – – – V_{in}, – – – – V_O) of the electronically controllable APF with different I_B values.

given by

$$s^2C_2C_3R_1R_2 + sC_3R_2 - sC_1R_1 + 1 = 0 \tag{21}$$

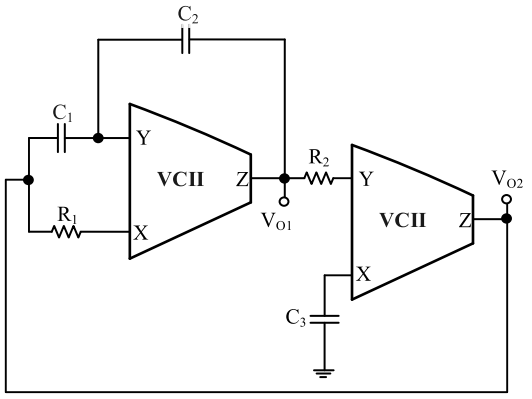


FIGURE 29. Quadrature oscillator.

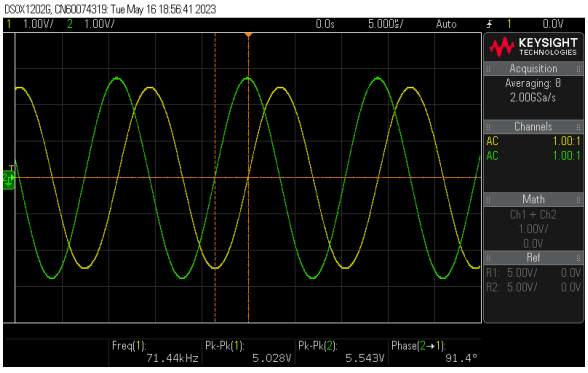


FIGURE 30. Measured sinusoidal output waveforms (– – – – V_{O1}, – – – – V_{O2}).

From (21), the frequency and condition of the proposed oscillator are given by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C_2C_3R_1R_2}} \tag{22}$$

and

$$C_1R_1 \geq C_3R_2 \tag{23}$$

The output voltages, V_{O2} and V_{O1}, are given by

$$V_{O2}(t) = V_{m2}Cos\,(2\pi f_0 t) \tag{24}$$

$$V_{O1}(t) = V_{m1}Cos\left(2\pi f_0 t - 90^\circ\right) = V_{m1}Sin\,(2\pi f_0 t) \tag{25}$$

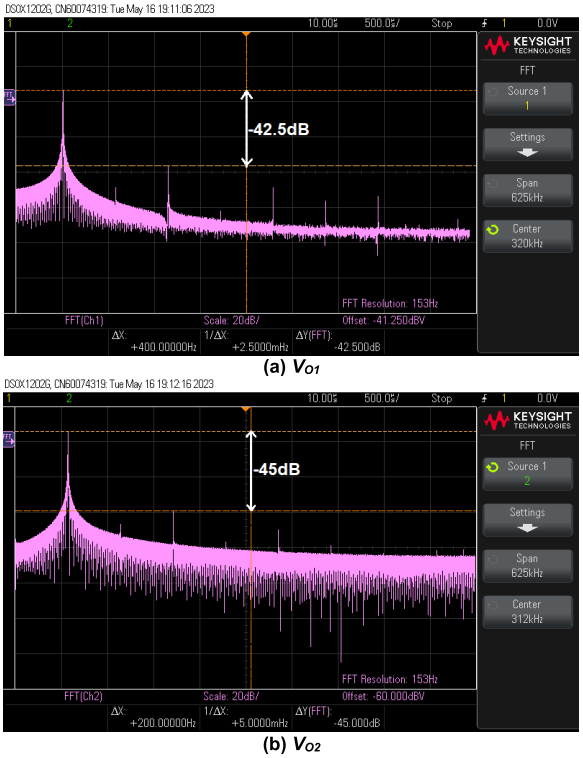
From (24) and (25), the phase difference of the sinusoidal output voltages, V_{O1} and V_{O2} is 90 degrees, where the phase of V_{O2} leads phase of V_{O1}. V_{m1} and V_{m2} are amplitudes of the $V_{O1}(t)$ and $V_{O2}(t)$, respectively.

The quadrature sinusoidal oscillator is tested by experiment verification utilizing the AD844-based VCII. Figure 30 displays the experimental results of the quadrature sinusoidal waveforms, V_{O1} and V_{O2} where $C_1 = C_2 = C_3 = 1$nF, R_1 =2.3kΩ, R_2 =2kΩ and ±5 supply voltages. The experimental results revealed that the experimental frequency of oscillation is 71.44kHz and the experimental phase difference between V_{O2} and V_{O1} is 91.40°. The theoretical frequency of oscillation calculated from (22) is 74.21kHz. So, the percentage error of the experimental frequency of

TABLE 7. Comparison of the proposed first-order filter with previous works.

Parameters	[19] Fig. 17	[29] Fig. 18B	[30] Fig. 5	[31]	[35]	[36]	[37]	This work
Technology	AD844	0.18 µm	0.35µm	0.18 µm	0.18 µm	0.13 µm	0.18 µm	0.18 µm
Supply voltage [V]	-	±0.9	±1.65	±0.9	0.5	±0.9	±0.9	±0.2
No. of ABB	2 VCII	1 VCII	1 VCII	2 VCII	2 OTA	1 CFOA, 1 UGIA	1 VGA	1 VCII
There is no need for multiple outputs or different types of ABB.	No	Yes	Yes	No	Yes	Yes	No	Yes
No. of passive element	4	2	3	4	1	2	2	3
Low output voltage impedance	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Availability of responses	LPF	LPF	LPF	APF	LPF, HPF, APF	LPF, HPF, APF	LPF, HPF, APF	LPF, HPF, APF
Power consumption	-	-	0.7mW	1.22mW	59.5nW	980µW	1.31mW	383nW
THD	<1.2% @2V_{pp}	-	<1.49% @20mV_{pp}	<3% @45µA	0.36% @40mV_{pp}	1% @120mV_{pp}	0.15% @40mV_{pp}	0.34% @300mV_{pp}
Dynamic range (dB)	-	-	-	-	-	-	-	72.9
Verification of result	Exp.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim./Exp.	Sim.

* Notes: Performance comparison is obtained through simulation, except in [19]. UGIA is a unity gain-inverting amplifier.



(a) V_{O1}

(b) V_{O2}

FIGURE 31. The measured output spectrum of V_{O1} and V_{O2}.

oscillation is 3.73%. The percentage error of the phase difference between V_{O2} and V_{O1} is 1.55%. Figure 31 illustrates the measured output spectrum of quadrature sinusoidal waveforms, V_{O1} and V_{O2}, when the total harmonic distortions of V_{O1} and V_{O2} are 0.75% (-42.50dB) and 0.56% (-45dB), respectively.

VII. CONCLUSION

In this paper, a VCII-based first-order multifunction filter is proposed. The proposed filter utilizes a single VCII and three passive elements. Two types of first-order filters are reconfigurable. The first type with a VCII, two resistors, and one capacitor can provide three first-order filtering functions, inverting LPF, non-inverting HPF, and inverting APF (leading phase). The second type with a VCII, two capacitors, and one resistor can also provide three first-order filtering functions: non-inverting LPF, inverting HPF, and non-inverting APF (lagging phase). The proposed filter has a low output impedance, which can be easily cascaded in voltage-mode circuits. The effect of voltage/current gain errors and parasitic elements in VCII is also studied, which reveals the importance of this phenomenon for the proposed second type of filter. Moreover, the second type of the proposed first-order APF is modified to achieve electronic controllability by replacing the passive resistor R with the OTA-based circuit. With this modification, the phase shift of the APF is electronically tuned. The proposed first-order filter has been simulated in the Cadence program using the 0.18μm CMOS technology from TSMC. Moreover, the proposed filter and its modification for electronic controllability are experimentally investigated using commercially available AD844 IC-VCII and LT1228-based OTA. Also, a quadrature sinusoidal oscillator based on the proposed type-2 first-order filter has been designed as an example of an application. The simulation and experimental results are in good agreement with the theoretical expectations.

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