IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 3 April 2024, accepted 12 April 2024, date of publication 15 April 2024, date of current version 30 April 2024.

*Digital Object Identifier 10.1109/ACCESS.2024.3389060*

RESEARCH ARTICLE

# 0.5-V High Linear Fully Differential Multiple-Input Bulk-Driven OTA With Effective Self-Embedded CMFB

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This work was supported by the University of Defence Brno within the Organization Development Project Military Autonomous and Robotic Assets (VAROPS).

**ABSTRACT** This paper presents a new fully differential multiple-input operational transconductance amplifier (FD MI-OTA) with an effective self-embedded common-mode feedback circuit (CMFB). The circuit employs several design techniques to extend the linearity to the rail-to-rail level, such as a bulk-driven, multiple-input capacitive voltage divider and source degeneration. The circuit uses self-cascode transistors to increase the gain of the OTA from one side and to create a common-mode feedback circuit, needed to control the common-mode output voltage from the other side. Thus, the CMFB is part of the OTA and as a result, its chip area and power consumption remain unchanged. The performance of the proposed circuit was simulated using TSMC's CMOS 0.18 $\mu$m process in the Cadence Virtuoso System Design Platform to validate the performance of the topology. Intensive simulation results based on Monte Carlo and process, voltage, temperature corners were performed to confirm the OTA's performance and the robustness of the CMFB. The circuit operates with a supply voltage of 0.5 V and consumes 17.5nW of power, making it suitable for applications with extremely low voltage supply and low frequency. As an application, a second-order low-pass filter was designed based on the proposed FD MI-OTA.

**INDEX TERMS** Universal filter, voltage-mode circuit, operational transconductance amplifier.

## I. INTRODUCTION

In modern nanoscale CMOS technology, the supply voltage ($V_{DD}$) decreases continuously to reduce the overall power dissipation and maintain circuit reliability. Therefore, circuit designers must develop new techniques to maintain analog circuit performance at extremely low supply voltages, even much lower than the threshold voltage ($V_{TH}$), i.e., $V_{DD} \leq V_{TH}$. Unlike digital circuits, the performance of analog circuits is strongly affected by the use of nanoscale technology and reduced supply voltages. Therefore, designing integrated circuits with extremely low-power consumption is now becoming crucial for various applications, especially in the context of battery or energy harvester powered devices, such as portable or biomedical wearable electronics, IoT (Internet of Things) devices, self-powered autonomous sensors, etc.

The operational transconductance amplifier (OTA) is a key building block in analog signal processing used to convert the input voltage signal into the output current signal. It has been widely used for instance in continuous-time delta-sigma modulators, voltage-controlled oscillators, multipliers, and OTA-C filters due to its transconductance controllability [1], [2], [3], [4], [5], [6].

The OTA with fully differential architecture (FD-OTA) provides advantages compared to the single ended OTA.

The associate editor coordinating the review of this manuscript and approving it for publication was Feng Lin.

Namely, it provides an improved output swing, linearity, common-mode rejection ratio and dynamic range. Therefore, the FD OTA's capabilities make it a versatile building block for a wide range of analog and mixed-signal circuit designs, particularly in applications that benefit from improved common-mode rejection and differential signal processing. These include audio amplifiers, analog filters, data converters (D/A and A/D), modulators, instrumentation, etc. [7]. However, the FD-OTA requires a common-mode feedback circuit (CMFB) to ensure that the common-mode output voltage ($V_{o-cm}$) is within a desired range, usually around the mid supply, i.e. ($V_{o-cm} = (V_{DD}\text{-}V_{SS})/2$). This is because the output common-mode level is very sensitive to device properties and mismatches and cannot be precisely defined in the presence of differential feedback [7].

The CMFB typically uses passive resistors and/or active blocks like operational amplifiers to sense the CM output level of the FD-OTA. Thus, it can generate feedback signals to the main FD-OTA to correct the CM output voltage and bring it closer to the desired CM value. Although the CMFB is necessary for the proper operation of the FD-OTA, it increases circuit complexity, chip area, and power consumption. To reduce this problem, simple implementations of embedded CMFB circuits were proposed, using transistors operating in the triode region [8], [9]. However, these structures are not suitable for ultra-low voltage supply, i.e. $V_{DD} \leq V_{TH}$. FD-OTA structures with low-voltage operation capability ($V_{DD} = V_{TH} = 0.5V$) are presented in [10], [11], and [12]. These structures simply use self-cascode transistors (SC) as a CMFB; hence, no extra power dissipation or chip area are needed. However, these structures use only one-sided SC CMFB (i.e. PMOS SC), which results in an 80% accuracy of $V_{o-cm}$. In this paper, in order to increase the accuracy up to 99.6%, we introduce the novel CMFB that embedded in SC of both side of the FD-OTA structure (i.e. NMOS and PMOS SC) to control and adjust the CM output voltage. In this way, we achieve an effective and self-embedded CMFB suitable for low-voltage supply without a need for an increase in chip area or power dissipation. In other words, the circuit simply took advantage of the bulk-terminal as a control gate to set the proper CM output voltage, Therefore, there is no additional circuity required for the CMFB, nor is there any chip area or power consumption.

This paper presents the FD MI-OTA that employs several design techniques suitable for extremely low-voltage supply and low frequency applications. The paper is organized as follows: in Section II, the CMOS structure of the FD MI-OTA is described, and an example of the filter's application is provided. In Section III, detailed simulations of the CMOS structure and the filter are presented. Finally, conclusions are given in Section IV.

## II. CIRCUIT DESCRIPTION

### A. FULLY DIFFERENTIAL MULTIPLE-INPUT OTA

Fig. 1 shows the electrical symbol of the fully differential multiple-input OTA. Its ideal characteristics can be expressed by:

$$I_o = I_{o+} - I_{o-} = \sum_{i=1}^{N} g_m (V_{+i} - V_{-i}) \tag{1}$$

The CMOS implementation of the FD MI-OTA is shown in Fig. 2. The circuit can be considered as a current-mirror OTA with a linearized bulk-driven (BD) input stage, and multiple input, realized using a capacitive voltage summing circuit, consisting of the capacitors $C_{B1}$-$C_{B4}$. The core of the BD input stage (transistors $M_1$, $M_2$, $M_{11}$, $M_{12}$ biased by the current mirrors $M_9$-$M_{10}$) exploits the linearization principle. This is first described in [13] for conventional gate-driven (GD) circuits operating in strong inversion, and then adapted to weakly inverted BD transistors in [14].

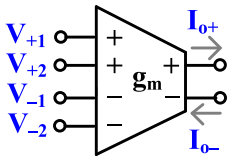


**FIGURE 1.** Electrical symbol of the FD MI-OTA.

The large signal transfer characteristic of the input stage, from the bulk terminals of $M_1$ and $M_2$, with $I_{D9} = I_{D10} = I_{set}$, can be described as [14]:

$$I_{D1} - I_{D2} = 2I_{set} tanh\left(\eta \frac{V_{bi}}{2n_p U_T} - tanh^{-1} \times \left[\frac{1}{4m+1} tanh\left(\eta \frac{V_{bi}}{2n_p U_T}\right)\right]\right) \tag{2}$$

where $\eta = (n_p\text{-}1)=g_{mb1,2}/g_{m1,2}$ is the bulk to gate transconductance ratio at the operating point for the input transistors $M_1$ and $M_2$, $n_p$ is the subthreshold slope factor for p-channel devices, $U_T$ is the thermal potential, $m=(W_{11,12}/L_{11,12})/(W_{1,2}/L_{1,2})$ is the relative aspect ratio of the two matched transistor pairs $M_{11,12}$- $M_{1,2}$, and $V_{bi} = V_{B2}$-$V_{B1}$ is the differential voltage between the bulk terminals of $M_2$ and $M_1$.The optimum linearity performance is obtained for m=0.5 [14].

In order to realize the MI-OTA, an additional voltage divider/summing circuit composed of the capacitors $C_{B1}$-$C_{B4}$ has been added in the considered design. Such a solution simplifies the overall structure and decreases the dissipation power of the MI-OTA, since additional active differential stages can be avoided. Moreover, the linear range of the OTA can be extended due to the voltage attenuation introduced by the input capacitive divider. The large resistors, composed of the transistors $M_{b1}$, $M_{b2}$, operating in the cut-off region with $V_{GS} = 0$, provide proper biasing of the bulk terminals of the input transistors $M_1$, $M_2$ for dc. Since they are connected to $V_{DD}$, the input transistors $M_1$ and $M_2$ operate with $V_{BS} > 0$ at operating point. This decreases the input currents of their bulk terminals and increases the input resistance of the OTA. Note that non-zero input currents are one of the most important problems in BD circuits, especially at higher temperatures.

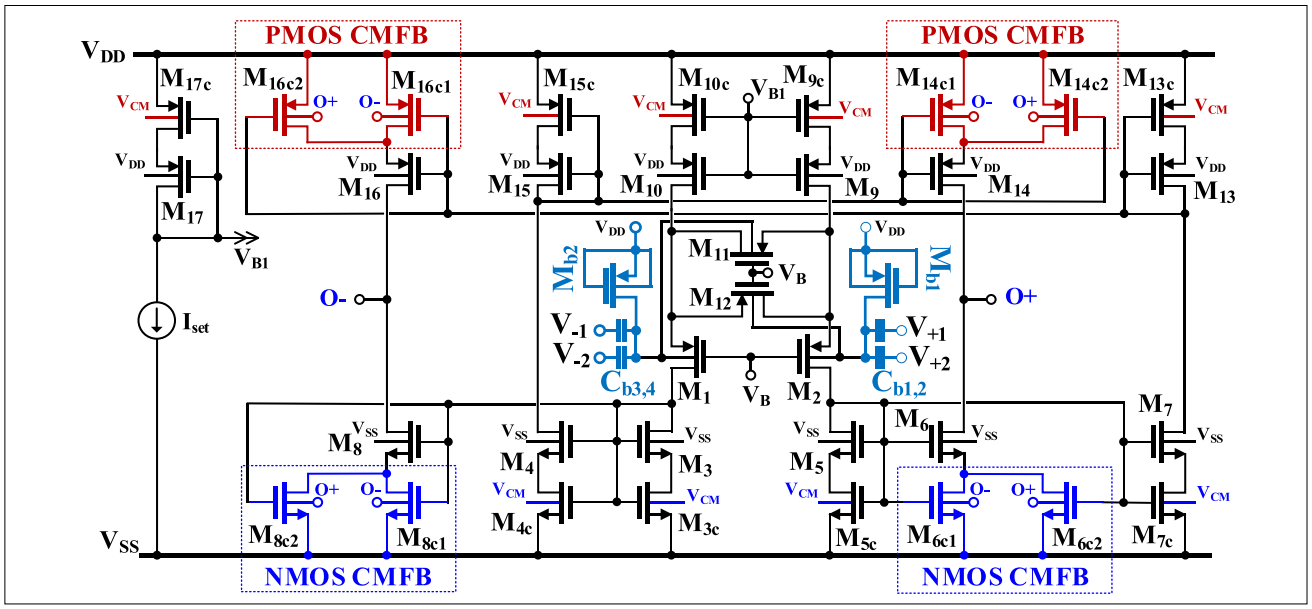


**FIGURE 2.** The proposed CMOS structure of the multiple-input FD-OTA with effective and self-embedded CMFB.

It is also worth noting that the application of only one resistor, common for all inputs, distinguishes this solution from the one used in [14].

The input capacitances, together with the biasing resistors $M_{b1,2}$, form a high-pass filter with the cut-off frequency $\omega_c = 1/C_\Sigma R_{LARGE}$, where $C_\Sigma$ is the sum of all capacitors $C_{Bi}$ at one side (e.g. $C_{B1} + C_{B2} = C_{B3} + C_{B4}$ in Fig. 2), and $R_{LARGE}$ is the resistance of the biasing resistors $M_{b1,2}$ at the operating point. Due to the very large value of $R_{LARGE}$, a cut-off frequency in the range of several hertz can be obtained, even for capacitors with capacitances less than 1pF.

Neglecting the input impedance of the OTA core, and assuming that all input capacitances $C_{Bi}$ are identical, the input differential ac voltage at the bulk terminals of $M_1$ and $M_2$, for N inputs, can be expressed as:

$$V_{bi} = \frac{1}{N}[(V_{+1} + V_{+2}) - (V_{-1} + V_{-2})] \tag{3}$$

thus, the multiple input function, as described by (1), is realized. From (2) and (3), assuming unity-gain current mirrors $M_4$-$M_8$ and $M_6$-$M_7$, the small-signal trans-conductance of the OTA can be expressed as:

$$g_m = \frac{\eta}{N} \cdot \frac{4m}{4m+1} \cdot \frac{I_{set}}{n_p U_T} \tag{4}$$

For the optimum case (m=0.5) and N=2 as in Fig. 2, the transconductance can be calculated as:

$$g_m = \frac{\eta}{3} \cdot \frac{I_{set}}{n_p U_T} \tag{5}$$

Since the input capacitive divider attenuates the input ac signal N times, the linear range of the OTA is increased N times as well; however, its transconductance is decreased in the same proportion. It is also worth mentioning that input

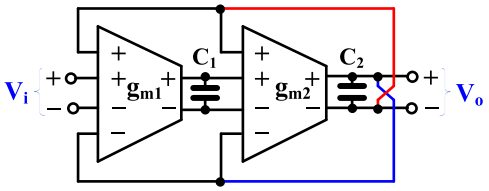


**FIGURE 3.** Proposed second order voltage-mode low-pass filter using FD MI-OTAs.

**TABLE 1.** Parameters of the components of the MI-OTA.

| Transistor | W/L (μm/ μm) |
|---|---|
| $M_1$, $M_2$, $M_3$-$M_8$, $M_9$, $M_{10}$, $M_{13}$-$M_{17}$ | 2×15/1 |
| $M_{11}$, $M_{12}$ | 15/1 |
| $M_{3c}$-$M_{5c}$, $M_{7c}$ | 2×1/2 |
| $M_{6c1}$, $M_{6c2}$, $M_{8c1}$, $M_{8c2}$ | 1/2 |
| $M_{9c}$, $M_{10c}$, $M_{13c}$, $M_{15c}$, $M_{17c}$ | 2×2/2 |
| $M_{14c1}$, $M_{14c2}$, $M_{16c1}$, $M_{16c2}$ | 2/2 |
| $M_{b1}$, $M_{b2}$ | 4/5 |
| $V_B$=-80mV, $C_{b1\text{-}4}$=0.5pF | |

referred noise is also increased N times; therefore, the input capacitive divider does not affect the dynamic range of the OTA. However, it simplifies its structure.

The current mirrors used in the structure are based on the so-called self-cascode transistors, a technique often used in ULV circuits to enlarge the output resistance of the OTA, and consequently its low-frequency voltage gain, while not limiting its output voltage swing.

The low-frequency voltage gain of the OTA, above $\omega_c$, can be approximated as:

$$A_V \cong g_m[(g_{m8} r_{dsD8} r_{ds8c}) \,||\, (g_{m16} r_{ds16} r_{ds16c})] \tag{6}$$

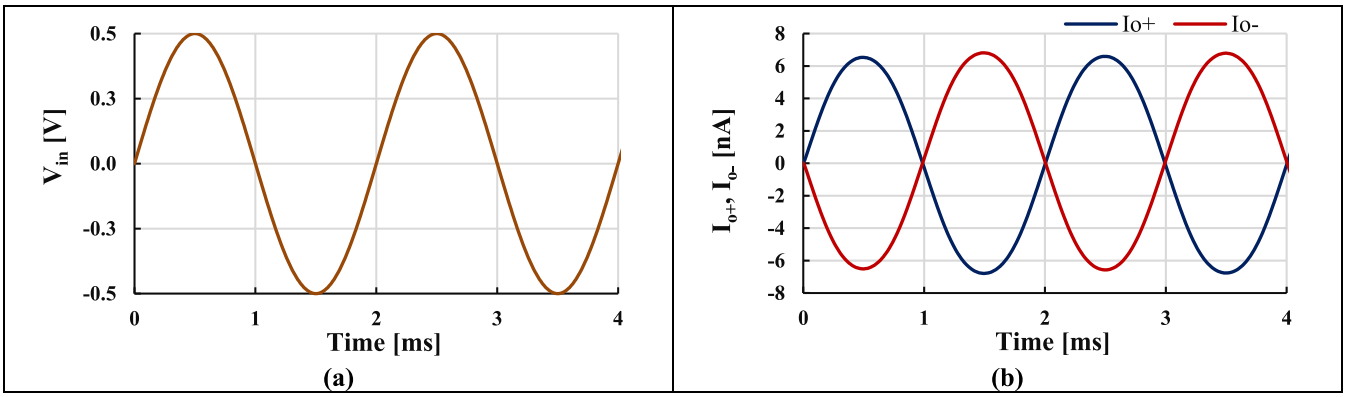


**FIGURE 4.** The transient characteristics the FD MI-OTA: (a) input applied voltage, (b) output currents $I_{o+}$ and $I_{o-}$.

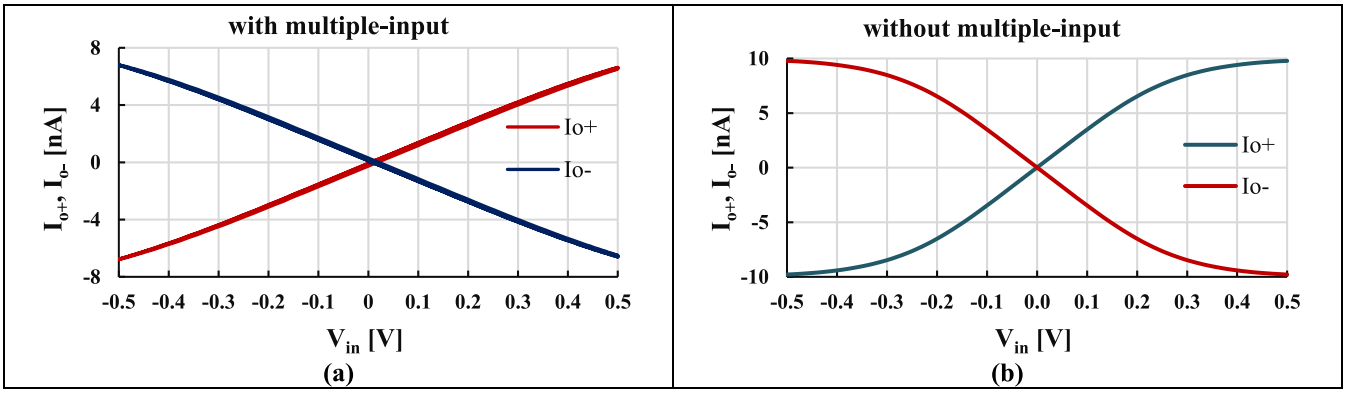


**FIGURE 5.** The transfer characteristics of the FD OTA: (a) with MI, (b) without MI.

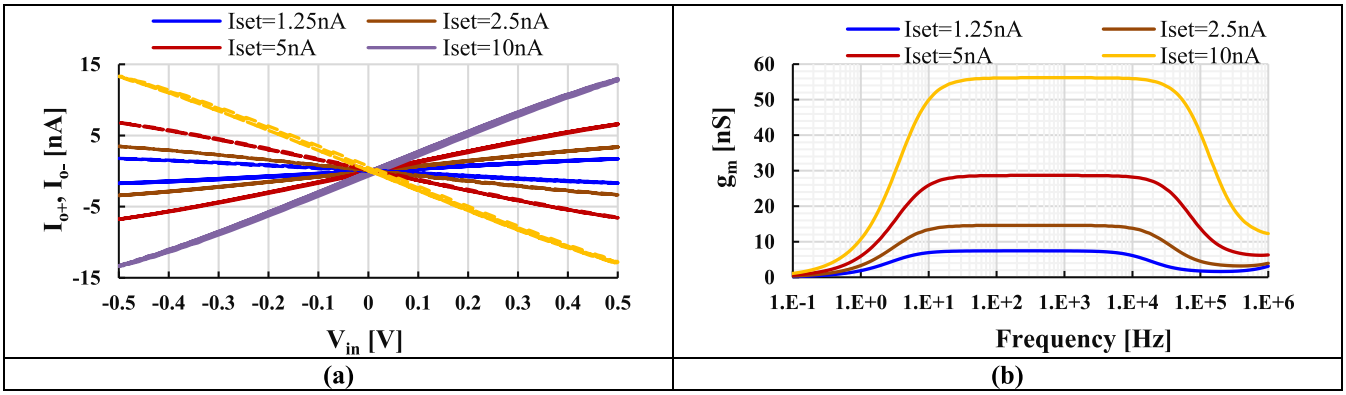


**FIGURE 6.** The transfer characteristics of the FD MI-OTA with different $I_{set}$: (a) output currents $I_{o+}$ and $I_{o-}$, (b) total transconductance $g_m$.

It is worth noting that some of the triode-region transistors $M_{ic}$ are split into two parts (i.e. with the same length L and half width W, so the total chip area remains the same) and their bulk terminals are connected to differential outputs of the OTA, or to the reference voltage $V_{CM}$. In this way, a common-mode feedback (CMFB) circuit is realized. Similar triode-region CMFBs have already been used in other works [10], [11], [12]. The novelty here is application of both p- and n-channel transistors. This provides better efficiency of the circuit, especially in an ultra-low voltage environment, where the voltage drops $V_{DS}$ across the triode region transistors $M_{ic}$ are strongly limited (ca. 15mV in the proposed design). Note that the bulk terminals of both types of MOS transistors are easily accessible in contemporary technologies. Such a solution also provides a lower nonlinear distortion introduced by the CMFB as compared to its single-polarity version.

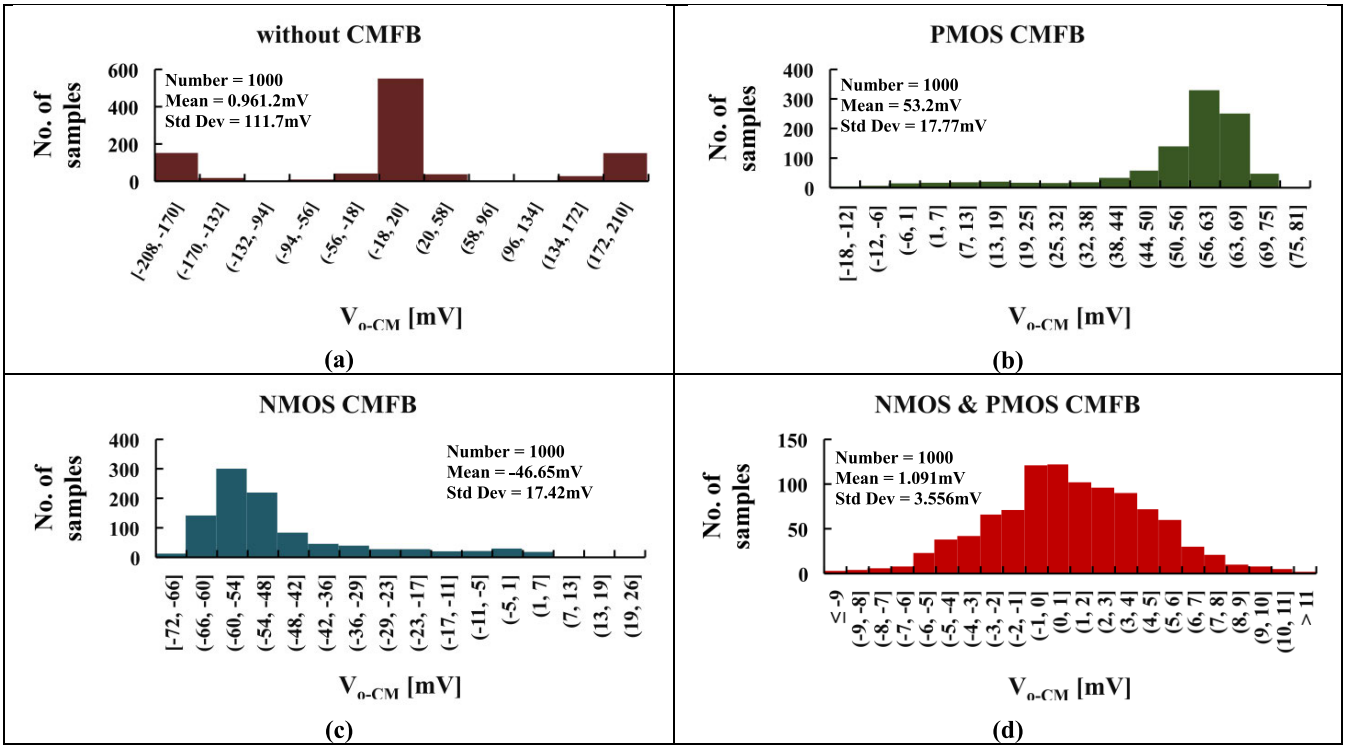


**FIGURE 7.** The CM output voltage with 1000 run Monte Carlo analysis: (a) without CMFB, (b) PMOS CMFB, (c) NMOS CMFB and (d) NMOS & PMOS CMFB.

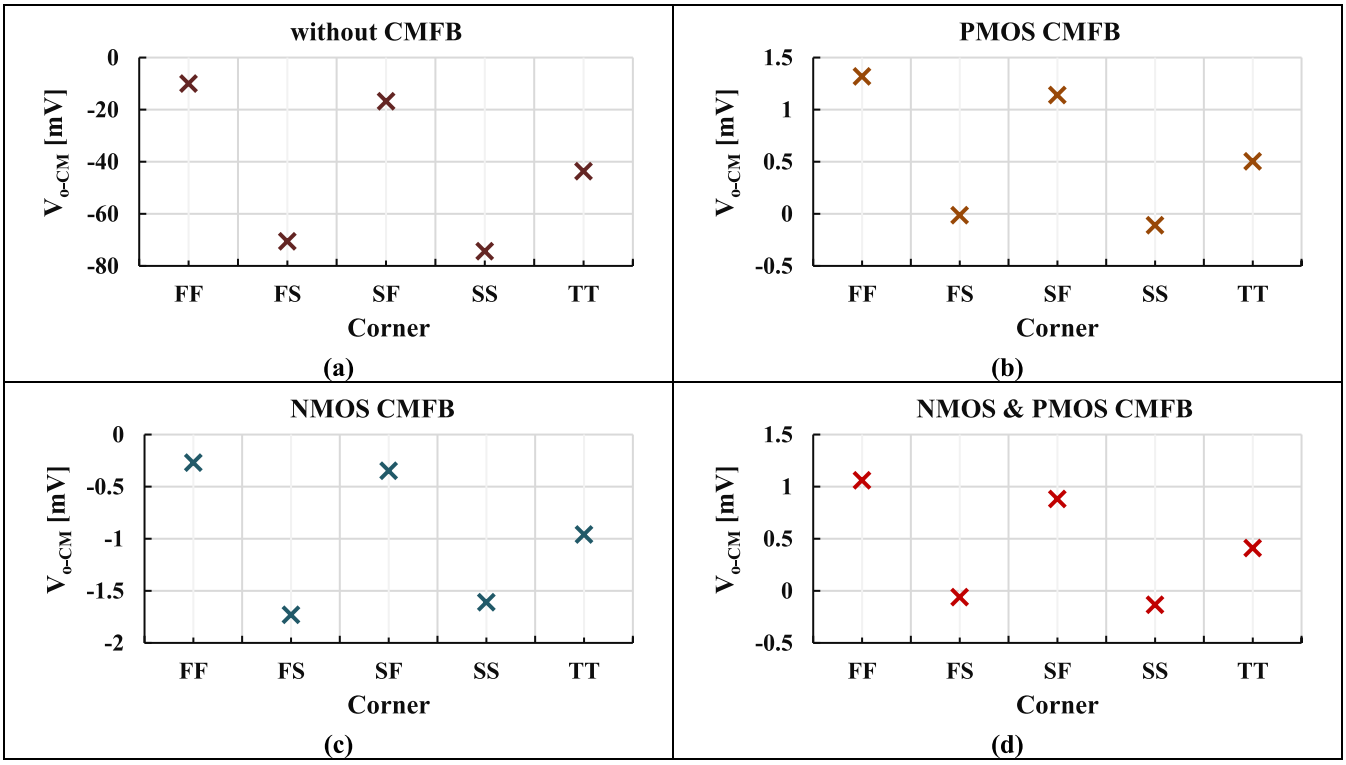


**FIGURE 8.** The CM output voltage with process corners analysis: (a) without CMFB, (b) PMOS CMFB, (c) NMOS CMFB and (d) NMOS & PMOS CMFB.

### *B. PROPOSED LOW PASS FILTER*

Fig. 3 shows the proposed second order voltage-mode low-pass filter using two FD MI-OTAs and two capacitors. The input and output are fully differential, which offers the advantages of improved voltage swings and dynamic range. It should be noted here that using a multiple-input OTA

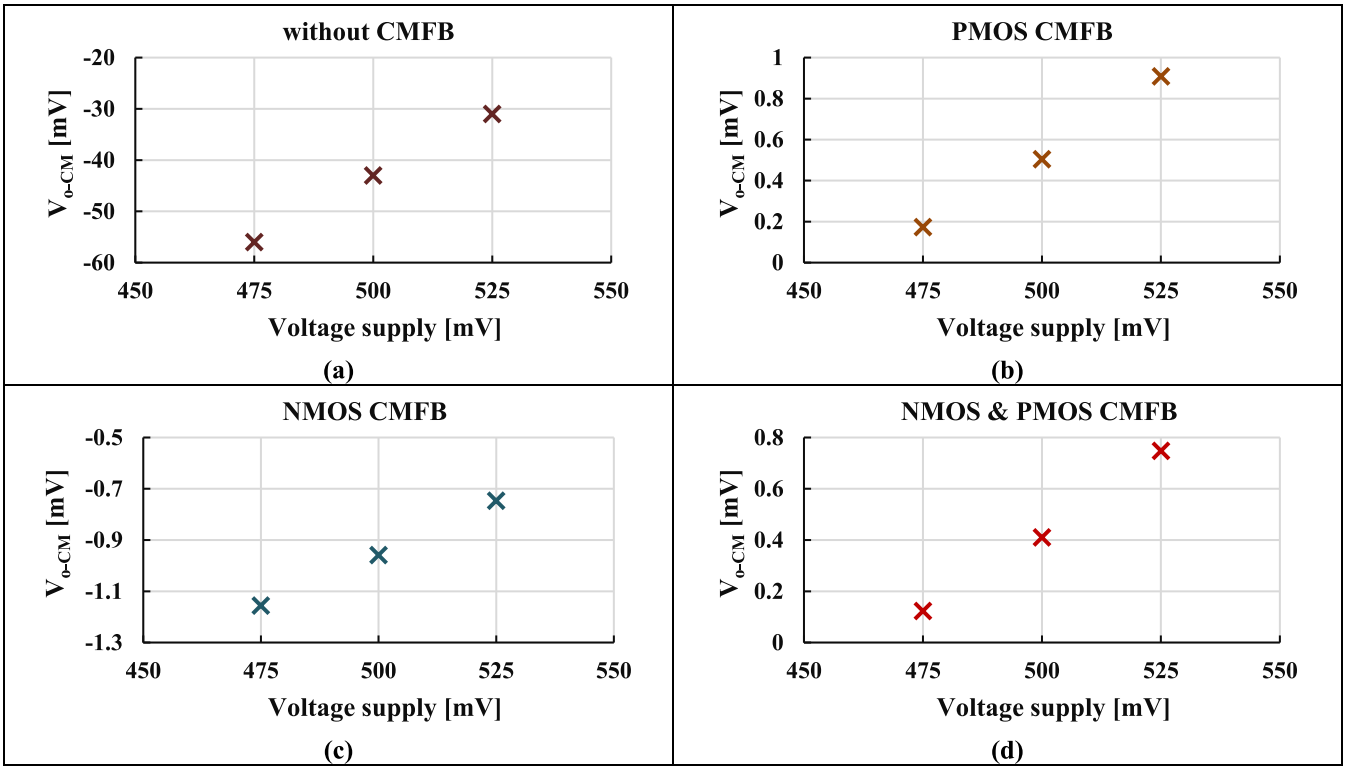


**FIGURE 9.** The CM output voltage with voltage supply corners analysis: (a) without CMFB, (b) PMOS CMFB, (c) NMOS CMFB and (d) NMOS & PMOS CMFB.

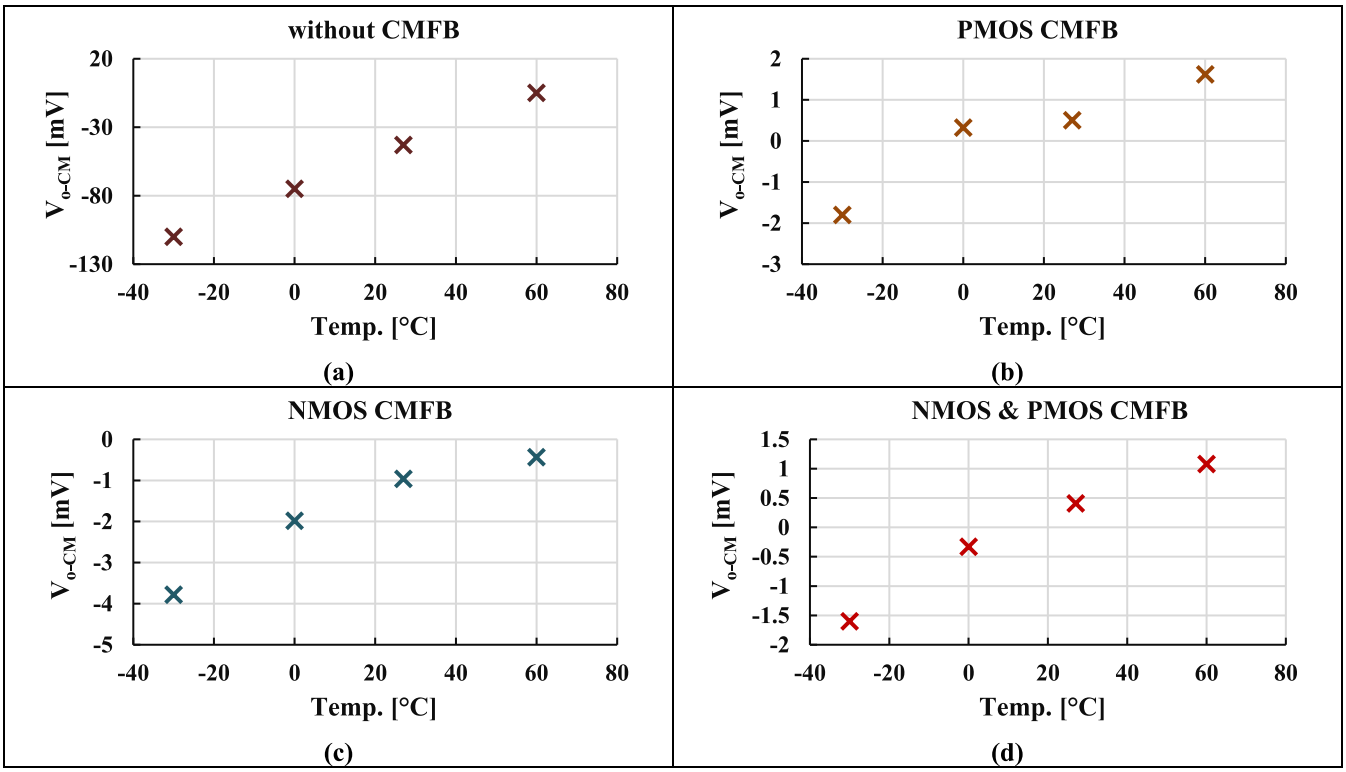


**FIGURE 10.** The CM output voltage with temperature corners analysis: (a) without CMFB, (b) PMOS CMFB, (c) NMOS CMFB and (d) NMOS & PMOS CMFB.

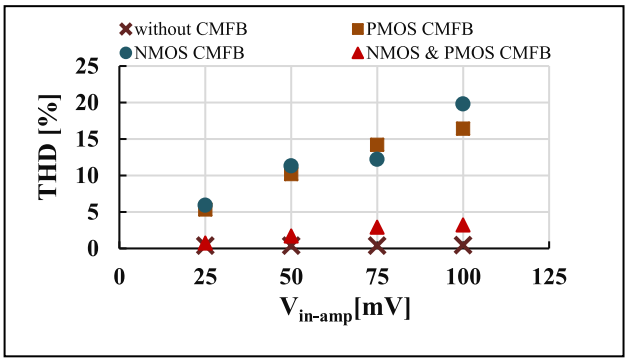


**FIGURE 11.** The THD of the FD MI-OTA with different CMFBs.

reduces the number of active blocks required to implement the filter compared to using a conventional OTA.

Neglecting second-order effects, the transfer function of the circuit in Fig. 3 is given by:

$$\frac{V_o}{V_i} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + \frac{g_{m2}}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2}} \tag{7}$$

Hence, the natural frequency ($\omega_o$) and the quality factor ($Q$) can be expressed by:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{8}$$

$$Q = \sqrt{\frac{g_{m1}C_2}{g_{m2}C_1}} \tag{9}$$

## III. SIMULATION RESULTS

The proposed FD MI-OTA and the filter application were simulated in the Cadence Virtuoso System Design Platform using 0.18$\mu$m CMOS technology from TSMC (Taiwan Semiconductor Manufacturing Company). The aspect ratio of the MOS transistors of the FD MI-OTA in Fig. 2 is listed in Table 1. The voltage supply was 0.5 V ($V_{DD} = -V_{SS} =$ 0.25V). The proposed MI-OTA consumes 17.5nW for a 5nA setting current.

Due to the limited voltage headroom, possible PVT variations, signal swing and to maximize tuning range of the OTA, for compensating possible variations of gm, it is very important to assume proper values of $V_{GS}$ voltages of all transistors, that provide maximum possible variations of $V_{GS}$ without changing the assumed region of operation. Because (treating the SC structure as one transistor) there are 3 transistors stacked from $V_{SS}$ to $V_{DD}$ in the input stage, we assumed $V_{GS}$ of all transistors in the circuit equal to ca. 167 mV, i.e. 1/3 of the applied supply voltage. Then we assumed a relatively large channel lengths of all transistors, L=1$\mu$m, to maximize their output resistances $r_{ds}$ and consequently the dc voltage gain of the OTA. For the assumed nominal biasing current of 5nA, which was determined from (5) for the assumed nominal transconductance $g_m$, we determined the required values of the channel widths during the simulation phase to satisfy $V_{GS} \approx 167$mV. The aspect ratios of the triode-region transistors $M_{11}$ and $M_{12}$, were chosen to be equal a half of the aspect ratios of $M_{1,2}$, for optimum linearity, as mentioned previously. The W/L ratios of the triode region transistors with index "c" in self-cascode structures were determined to obtain $V_{DS}$ of 15mV for a nominal biasing current, i.e. the value much larger than possible variations of threshold voltages caused by mismatches, but still much lower than $4U_T$, which is a border between penthode and triode region. However, in order to obtain sufficient channel areas, and consequently to decrease the impact of mismatch, their L were finally increased during the simulation phase to 2$\mu$m. Note, that even with such L, their areas remained relatively low as compared with penthode-region transistors in SC structures. Finally, the W/L of $M_{b1}$ and $M_{b2}$ have been chosen during the simulation phase to provide sufficient $R_{LARGE}$.

The input high-pass filter prevents a DC analysis for the MI-OTA. Thus, the dynamic characteristic of the FD MI-OTA was obtained by applying a differential sine wave with an amplitude of 500 mV and frequency of 500 Hz to the input $V_{+1}$ and $V_{-1}$ of the FD MI-OTA, while the other inputs are connected to a common-mode voltage (0.25V), as shown in Fig. 4 (a). The output currents are shown in Fig. 4 (b). Fig. 5 (a) shows the MI-OTA transfer characteristics obtained from the transient analysis in Fig. 4. In order to demonstrate the advantage of the multiple-input, Fig. 5 (b) shows the DC characteristic of the FD OTA without multiple-input, i.e. the DC differential signal is applied directly to the bulk terminal of the input differential pair (i.e. neither $C_b$ nor $M_b$ are used). The extended linearity up to rail-to-rail is evident for the MI-OTA. The total harmonic distortion (THD) of the output currents in Fig. 4 (b) was 2.4%. The THD was below1% for the 370mV input amplitude at 500 Hz. The extended linearity of the MI-OTA with various setting currents $I_{set} =$ (1.25, 2.5, 5, 10)nA is shown in Fig. 6 (a), while the total transconductance AC characteristic is shown in Fig. 6(b). The transconductance was (7.4, 14.6, 28.7, 56.2)nS, respectively.

To demonstrate the effectiveness of the CMFB, the $V_{o-CM}$ was intensively investigated with Monte Carlo (MC) process and mismatch variations with 1000 runs and process, voltage, and temperature (PVT) corners analysis. The process corners for the transistor were fast-fast (FF), fast-slow (FS), slow-fast (SF), and slow-slow (SS). The voltage corners were ($V_{DD}$-$V_{SS}$)±10%, and the temperature corners were -30°C and 60 °C. The simulation results were provided for the proposed FD MI-OTA in Fig. 2 for the following cases:

a) without CMFB, i.e. the bulks of all SC PMOS and NMOS transistors are connected to $V_{DD}$ and $V_{SS}$, respectively.
b) with active SC PMOS CMFB, i.e. the SC NMOS CMFB is inactive, and their bulks are connected to $V_{SS}$.
c) with active SC NMOS CMFB (indicated in blue color), i.e. the SC PMOS CMFB is inactive, and their bulks are connected to $V_{DD}$.
d) with active SC NMOS & PMOS CMFBs (indicated in red and blue color).

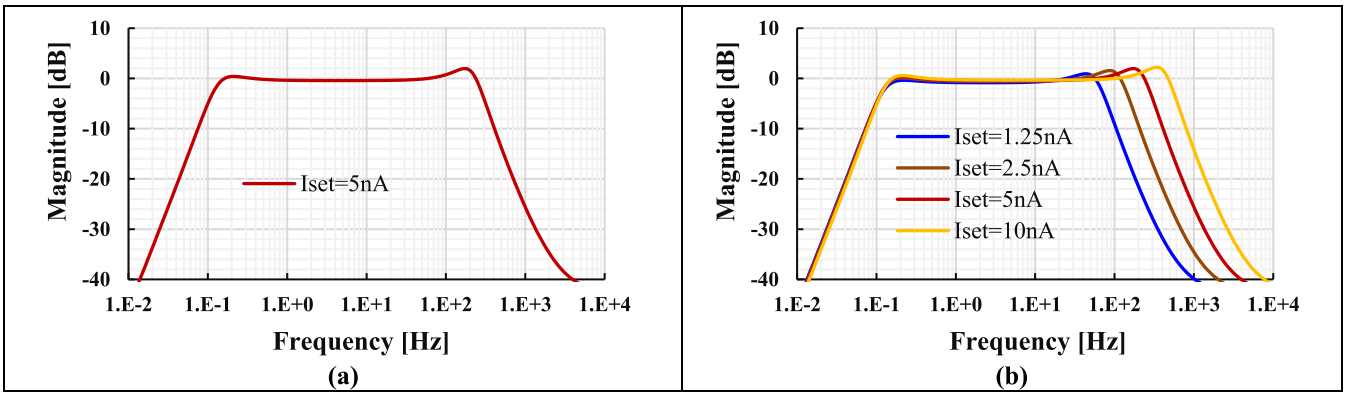


**FIGURE 12.** The frequency characteristics of the filter: (a) for $I_{set}$ = 5nA (b) with various $I_{set}$.

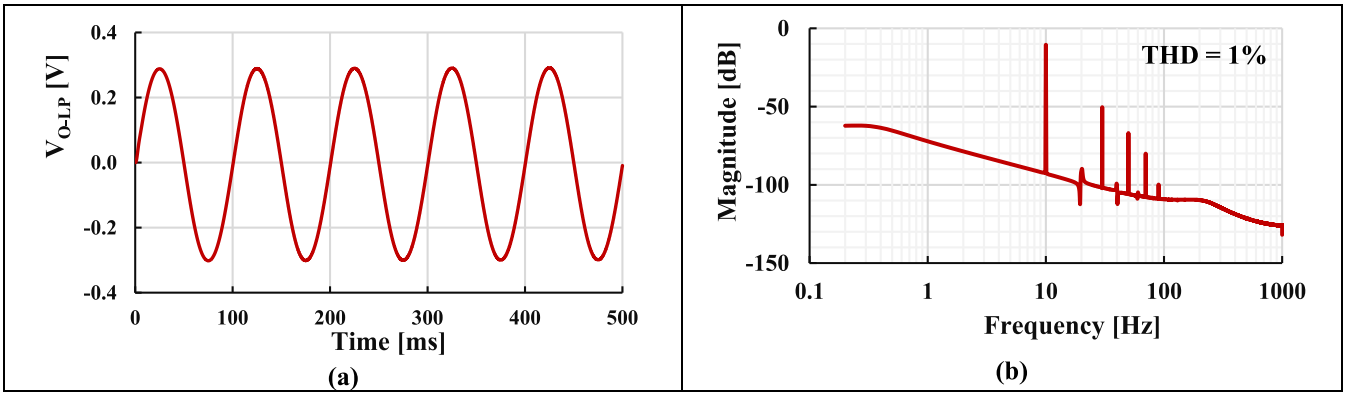


**FIGURE 13.** The transient characteristic of the BPF (a) and (b) the spectrum of the output signal.

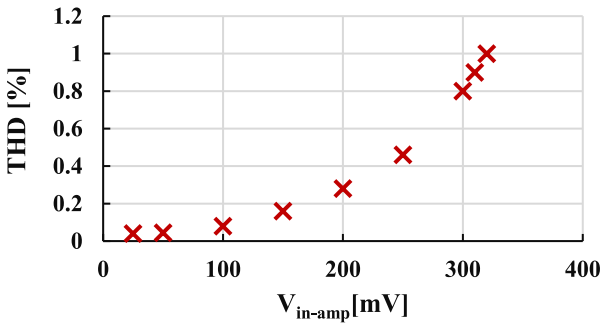


**FIGURE 14.** The THD versus the amplitude of the input signal.

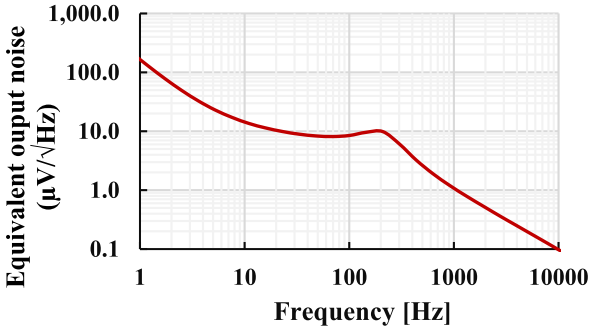


**FIGURE 15.** The equivalent output noise of the BPF.

As shown in Fig. 7, the MC analysis, the variance of the $V_{o-cm}$ without the CMFB is, as expected, unacceptably high, with a mean value of 0.961.2mV and standard deviation of 111.7mV. The variance of the $V_{o-cm}$ with the SC PMOS CMFB shows a positive mean value of 53.2mV and standard deviation of 17.77mV. The variance of the $V_{o-cm}$ with SC NMOS CMFB shows a negative mean value of -46.65mV and standard deviation of 17.42mV. The variance of the $V_{o-cm}$ with SC NMOS & PMOS CMFBs shows a mean value of 1.091mV and standard deviation of 3.556mV. This confirms the effectiveness of the SC NMOS & PMOS CMFBs. Figs. 8, 9, 10 show the process, voltage and temperature corners analysis, respectively, for the proposed circuit, again for the cases of a-d. By inspecting these figures, we can conclude that the worst variance of the $V_{o-cm}$ is for the circuit without CMFB, while the least variance is for the circuit with SC NMOS & PMOS CMFB.

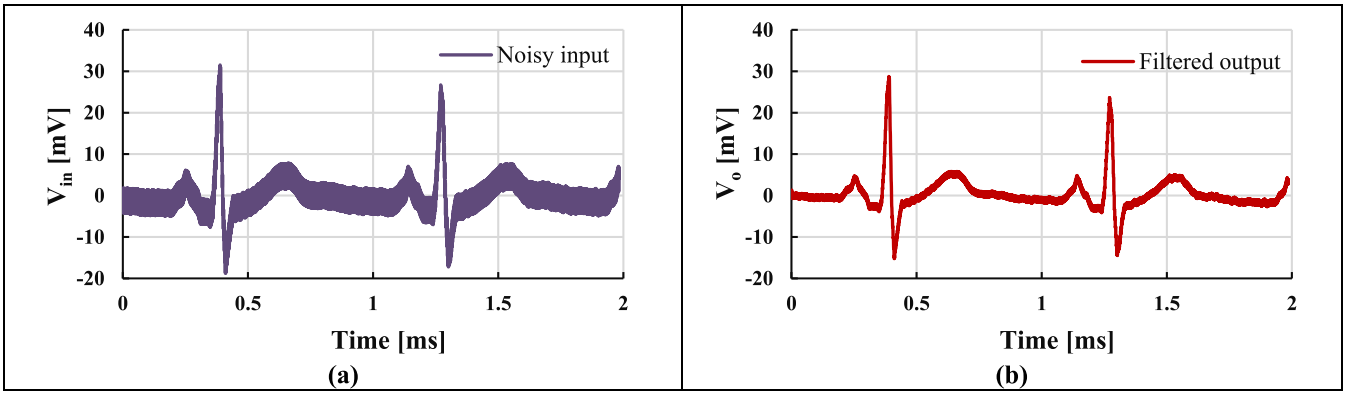


**FIGURE 16.** The transient characteristic of the LPF (a) noisy input signal and (b) filtered output signal.

**TABLE 2.** Performance comparison between the proposed filter and previous fifth-order low-pass filters.

| Symbol | This Work | IEEE TBioCAS (2009) [15] | IEEE TCAS-II (2018) [16] | IEEE TBioCAS (2019) [17] | IEEE ACCESS (2022) [18] | IEEE ACCESS (2023) [19] |
|---|---|---|---|---|---|---|
| $V_{DD}$ [V] | 0.5 | 1.0 | 1.0 | 1.0 | 0.5 | 1.0 |
| Tech [μm] | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | 0.065 |
| $V_{TH}$ [V] | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.3 |
| Order (N) | 2 | 5 | 5 | 5 | 5 | 5 |
| Filter type | Butterworth | Butterworth | Butterworth | Butterworth | Chebyshev | Butterworth |
| No. of active device | 2 FD MI-OTAs | 11-OTAs | 6 OTAs | 6 OTAs | 5 MI-OTAs | 11 OTAs |
| Architecture | $G_m$-C fully diff. | $G_m$-C fully diff. | $G_m$-C fully diff. | $G_m$-C fully diff. | $G_m$-C single-end | $G_m$-C fully diff. |
| MOST technique | MIBD | GD | GD | GD | MIBD | GD |
| Self-embedded CMFB circuit | Yes | No | No | No | - | No |
| CMOS structure complexity | Low | High | High | High | - | High |
| BW [Hz] | 290 | 250 | 250 | 250 | 250 | $1\times10^6$ |
| DR [dB] | 45.29 | 50 | 49.9 | 61.2 | 57.6 | 50.54 |
| Power (P) [nW] | 35 | 453 | 350 | 41 | 50 | $167\times10^3$ |
| Low voltage operation capability = $V_{TH}/V_{DD}$ * 100 [%] | 100 | 50 | 50 | 50 | 100 | 30 |
| Area [$mm^2$] | NA | 0.13 | 0.12 | 0.14 | 0.036 (off chip cap.) | 0.0164 |
| Obtained results | Simulated | Measured | Measured | Measured | Post-layout | Measured |

Note: MIBD = Multiple-Input Bulk-Driven, GD = Gate-Driven

Fig. 11. shows the THD of the proposed FD MI-OTA's output voltage signal with a load resistance of 100MΩ (i.e., the gain was 1.3×) and with an applied input sine wave signal with different amplitudes at 500Hz. The results clearly show that the SC NMOS & PMOS CMFB offers much less THD compared with SC NMOS CMFB or PMOS CMFB.

The frequency characteristic of the filter with $I_{set} = I_{set1,2} = 5nA$ and $C_1 = 8.15pF$, $C_2 = 13.93pF$ is shown in Fig. 12 (a). The low and high cutoff frequencies were 110mHz and 290 Hz, respectively. To demonstrate the tuning capability of the filter, Fig. 12 (b) shows its frequency characteristic for $I_{set} = (1.25, 2.5, 5, 10)nA$. The high cutoff frequencies were (75, 146, 290, 575) Hz, respectively.

The transient response of the filter's output signal with $I_{set} = 5nA$ and an applied input sine wave with an input amplitude of 320mV at 10Hz is shown in Fig. 13 (a). The spectrum of the output signal indicates 1%THD as shown in Fig. 13 (b). The THD versus the amplitude of the input signal at 10Hz is shown in Fig. 14.

The equivalent output noise is shown in Fig. 15. The root mean square (RMS) value of the output noise integrated in the passband of the filter was 1.23mV. The dynamic range was calculated as 45.29dB for 1% THD. The total power consumption of the filter was 35nW for a 5nA setting current.

The proposed filter was simulated to demonstrate its performance in processing electrocardiography (ECG) signals. Low (3mV at 10mHz) and high (3mV at 500Hz) frequency components were added to the clean the ECG signal, as shown in Fig. 16 (a). Fig. 16 (b). shows the output filtered signal.

Table 2 compares the proposed low-pass filter with some previous works. The fifth-order low-pass filters in [15], [16], [17], [18], and [19] have been selected for comparison. It clears that the FD MI-OTA based filter offers low-power consumption and low-voltage operation capability. The proposed filter further is the only one with self-embedded CMFB circuit which decreases the complexity of the CMOS design and prevents extra power dissipation and chip area.

## IV. CONCLUSION

In this paper, a new FD MI-OTA with an effective and self-embedded CMFB is presented. The CMFB is implemented to the SC PMOS and NMOS transistor to achieve high accuracy of the desired $V_{o-CM}$ around 99.6% without an increase in chip area or power dissipation. Intensive simulation results of MC and PVT analysis were carried out to confirm the performance and robustness of the design. The circuit is capable of operating with extremely low supply voltages ($V_{DD} = V_{TH} = 0.5V$) and offers an input voltage range up to rail-to-rail. The main concept of the proposed CMFB circuit is that the proposed OTA does not need any additional chip area. The circuit uses transistors already existing in the self cascode structure to increase the output resistance of the OTA, which have been divided into two parts. The bulk terminals of these transistors are used as a CMFB circuit. Therefore, there is no additional circuity required for the CMFB, nor is there any chip area or power consumption. The circuit simply took advantage of the bulk-terminal as a control gate to set the proper CM output voltage. This bulk terminal is not normally used in the standard design and is connected to $V_{DD}$ or $V_{SS}$ for PMOS and NMOS, respectively. This CMFB circuit principle can be applied to all OTA structures that use self-cascode structure.

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